

## Currículum vitae

Impreso normalizado (DRAC)

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Número de hojas que contiene: 45

Nombre y apellidos: Jordi Cortadella Fortuny

Fecha: 2 de marzo de 2026

Firma: Cortadella, J.

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La persona firmante declara que son ciertos los datos que figuran en este currículum y asumen, en caso contrario, las responsabilidades que se deriven de las inexactitudes que en él constan.

Es necesario firmar en el margen de cada una de las páginas.

Este currículum se presenta sin perjuicio de que en el proceso de evaluación se pueda pedir a la persona interesada la ampliación y justificación de la información que contiene.

## 1. Datos personales

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### Apellidos y nombre

Cortadella Fortuny Jordi

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## 2. Situación profesional actual

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<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Centro</b>
<b>Departamento, sección, unidad</b> Departament de Ciències de la Computació	
<b>Categoría profesional actual</b> Catedrático/a de universidad	<b>Fecha de inicio</b> 09-11-1999
<b>Situación administrativa</b> Funcionario	
<b>Dedicación</b> Tiempo completo	<b>Especialización (códigos UNESCO)</b>
<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Departamento, sección, unidad</b>
<b>Categoría profesional actual</b> Delegat Del Rector Adjunt Al Vr.de Recerca	<b>Fecha de inicio</b> 07-06-2021
<b>Situación administrativa</b> Otros	<b>Dedicación</b> Tiempo completo
<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Departamento, sección, unidad</b>
<b>Categoría profesional actual</b> Delegat/da Del Rector Adjunt/a Al Vicerektorat de Recerca	<b>Fecha de inicio</b> 07-06-2021
<b>Situación administrativa</b> Otros	<b>Dedicación</b> Tiempo completo
<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Departamento, sección, unidad</b>
<b>Categoría profesional actual</b> Delegat/da Del Rector Adjunt Al Vr.de Recerca	<b>Fecha de inicio</b> 07-06-2021
<b>Situación administrativa</b> Otros	<b>Dedicación</b> Tiempo completo
<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Departamento, sección, unidad</b>
<b>Categoría profesional actual</b> Delegat/da Rector Adjunt/a Al Vr.de Recerca	<b>Fecha de inicio</b> 07-06-2021
<b>Situación administrativa</b> Otros	<b>Dedicación</b> Tiempo completo
<b>Institución / organismo / empresa</b> Universitat Politècnica de Catalunya	<b>Departamento, sección, unidad</b>
<b>Categoría profesional actual</b> Director/a Escola de Doctorat	<b>Fecha de inicio</b> 21-12-2021
<b>Situación administrativa</b> Otros	<b>Dedicación</b> Tiempo completo

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## 3. Formación académica

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<b>Estudios de grado / 1er ciclo / 1er i 2undo ciclo / 2undo ciclo</b>	<b>Centro</b>	<b>Fecha de obtención</b>
Llicenciat en Informàtica (B.S. in Computer Science)	Universitat Politècnica de Catalunya	30-06-1985
Master en Informàtica (M.S. in Computer Science)	Universitat Politècnica de Catalunya	15-02-1986

<b>Doctorat</b>	<b>Centro</b>	<b>Fecha de obtención</b>
DOCTOR INFORMÀTICA	Universitat Politècnica de Catalunya	26-07-1987

<b>Altres titulacions de postgrau</b>	<b>Centro</b>	<b>Fecha de obtención</b>
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#### 4. Actividades de carácter científico o profesional anteriores a la situación actual

<b>Categoría</b>	<b>Institución</b>	<b>Periodo</b>
Col·laborador (ETS)	Universitat Politècnica de Catalunya	01-10-1985 - 30-09-1987
Profesor/ra asociado/da	Universitat Politècnica de Catalunya	01-10-1987 - 31-05-1988
Titular de universidad	Universitat Politècnica de Catalunya	01-06-1988 - 08-11-1999
Director/a Departament	Universitat Politècnica de Catalunya	12-02-2013 - 31-01-2018

#### 5. Idiomas

<b>Idioma</b>	<b>Comprensión auditiva</b>	<b>Comprensión lectora</b>	<b>Expresión escrita</b>	<b>Expresión oral</b>	<b>Interacción oral</b>
Catalán	C2	C2	C2	C2	C2
Castellano	C2	C2	C2	C2	C2
Inglés	C1	C1	C1	C1	C1
Francés	B1	B2	A1	A1	A1

## A. Publicaciones y tesis

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### A.1 Artículos en revistas

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Bernasconi, A.; Ciriani, V.; Cortadella, J.; Costa, M.; Villa, T. **Area-driven Boolean bi-decomposition by function approximation.** *ACM transactions on design automation of electronic systems*. 2025. Volumen: 30. Número: 1, article 5. <<https://doi.org/10.1145/3698879>>

Lagostina, L.; Minnella, F.; Cortadella, J.; Casu, M.; Lazarescu, M.; Lavagno, L. **Mix & Latch: Comparison with state-of-the-art retiming on a RISC-V benchmark.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2024. Volumen: 43. Número: 7. Págs.: 2229 ~ 2233. <<https://doi.org/10.1109/TCAD.2024.3360314>>

Minnella, F.; Cortadella, J.; Casu, M.; Lazarescu, M.; Lavagno, L. **Mix & Latch: An optimization flow for high-performance designs with single-clock mixed-polarity latches and flip-flops.** *IEEE access*. 2023. Volumen: 11. Págs.: 35830 ~ 35840. <<https://doi.org/10.1109/ACCESS.2023.3265809>>

Teren, V.; Cortadella, J.; Villa, T. **Generation of synchronizing state machines from a transition system: a region-based approach.** *International journal of applied mathematics and computer science*. 2023. Volumen: 33. Número: 1. Págs.: 133 ~ 149. <<https://doi.org/10.34768/amcs-2023-0011>>

Shan, J.; Lazarescu, M.; Cortadella, J.; Lavagno, L.; Casu, M. **Fast energy-optimal multi-kernel DNN-like application allocation on multi-FPGA platforms.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2022. Volumen: 41. Número: 4. Págs.: 1186 ~ 1190. <<https://doi.org/10.1109/TCAD.2021.3076958>>

Vidal, A.; Cortadella, J.; Petit, J.; Galceran, M.; Martorell, F. **Multi-level dataflow-driven macro placement guided by RTL structure and analytical methods.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2021. Volumen: 40. Número: 12. Págs.: 2542 ~ 2555. <<https://doi.org/10.1109/TCAD.2020.3047724>>

Shan, J.; Lazarescu, M.; Cortadella, J.; Lavagno, L.; Casu, M. **CNN-on-AWS: Efficient allocation of multikernel applications on Multi-FPGA platforms.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2021. Volumen: 40. Págs.: 301 ~ 314. <<https://doi.org/10.1109/TCAD.2020.2994256>>

Shan, J.; Lazarescu, M.; Cortadella, J.; Lavagno, L.; Casu, M. **Power-optimal mapping of CNN applications to cloud-based Multi-FPGA platforms.** *IEEE transactions on circuits and systems II: express briefs*. 2020. Volumen: 67. Número: 12, article 9103067. Págs.: 3073 ~ 3077. <<https://doi.org/10.1109/TCSII.2020.2998284>>

Segarra, J.; Cortadella, J.; Gran, R.; Viñals, V. **Automatic safe data reuse detection for the WCET analysis of systems with data caches.** *IEEE access*. 2020. Volumen: 8. Págs.: 192379 ~ 192392. <<https://doi.org/10.1109/ACCESS.2020.3032145>>

Machado, L.; Cortadella, J. **Support-reducing decomposition for FPGA mapping.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2020. Volumen: 39. Número: 1. Págs.: 213 ~ 224. <<https://doi.org/10.1109/TCAD.2018.2878187>>

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Machado, L.; Roca, A.; Cortadella, J. **Robustness to voltage noise with ring oscillator clocks.** *IEEE transactions on nanotechnology.* 2019. Volumen: 18. Págs.: 374 ~ 384.  
<<https://doi.org/10.1109/TNANO.2019.2908946>>

Moreno, A.; Cortadella, J. **State-based encoding of large asynchronous controllers.** *IEEE access.* 2018. Volumen: 6. Págs.: 61503 ~ 61518. <<https://doi.org/10.1109/ACCESS.2018.2872678>>

Petit, J.; Roura, S.; Carmona, J.; Cortadella, J.; Duch, A.; Giménez, O.; Mani, A.; Mas, J.; Rodriguez, E.; Rubio, A.; San Pedro, J. de; Venkataramani, D. **Judge.org: characteristics and experiences.** *IEEE transactions on learning technologies.* 2018. Volumen: 11. Número: 3. Págs.: 321 ~ 333. <<https://doi.org/10.1109/TLT.2017.2723389>>

Jain, P.; Cortadella, J.; Sapatnekar, S. **A fast and retargetable framework for logic-IP-internal electromigration assessment comprehending advanced waveform effects.** *IEEE transactions on very large scale integration (VLSI) systems.* 2016. Volumen: 24. Número: 6. Págs.: 2345 ~ 2358.  
<<https://doi.org/10.1109/TVLSI.2015.2505504>>

Cortadella, J.; Galceran, M.; Kishinevsky, M.; Sapatnekar, S. **RTL synthesis: From logic synthesis to automatic pipelining.** *Proceedings of the IEEE.* 2015. Volumen: 103. Número: 11. Págs.: 2061 ~ 2075.  
<<https://doi.org/10.1109/JPROC.2015.2456189>>

Cannizzaro, M.; Beer, S.; Cortadella, J.; Ginosar, R.; Lavagno, L. **SafeRazor: Metastability-robust adaptive clocking in resilient circuits.** *IEEE transactions on circuits and systems I: regular papers.* 2015. Volumen: 62. Número: 9. Págs.: 2238 ~ 2247. <<https://doi.org/10.1109/TCSI.2014.2365878>>

Carmona, J.; Cortadella, J. **Process discovery algorithms using numerical abstract domains.** *IEEE transactions on knowledge and data engineering.* 2014. Volumen: 26. Número: 12. Págs.: 3064 ~ 3076.  
<<https://doi.org/10.1109/TKDE.2013.156>>

Cortadella, J.; Petit, J.; Gomez, S.; Moll, F. **A boolean rule-based approach for manufacturability-aware cell routing.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2014. Volumen: 33. Número: 3. Págs.: 409 ~ 422. <<https://doi.org/10.1109/TCAD.2013.2292514>>

Cortadella, J. **Area-optimal transistor folding for 1-D gridded cell design.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2013. Volumen: 32. Número: 11. Págs.: 1708 ~ 1721.  
<<https://doi.org/10.1109/TCAD.2013.2269680>>

Nikitin, N.; San Pedro, J. de; Cortadella, J. **Architectural exploration of large-scale hierarchical chip multiprocessors.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2013. Volumen: 32. Número: 10. Págs.: 1569 ~ 1582. <<https://doi.org/10.1109/TCAD.2013.2272539>>

Peper, F.; Lee, J.; Carmona, J.; Cortadella, J.; Morita, K. **Brownian circuits: fundamentals.** *ACM journal on emerging technologies in computing systems.* 2013. Volumen: 9. Número: 1. Págs.: 3:1 ~ 3:24.  
<<https://doi.org/10.1145/2422094.2422097>>

Galceran, M.; Gotmanov, A.; Cortadella, J.; Kishinevsky, M. **Microarchitectural transformations using elasticity.** *ACM journal on emerging technologies in computing systems.* 2011. Volumen: 7. Número: 4. Págs.: 1 ~ 24.  
<<https://doi.org/10.1145/2043643.2043648>>

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Carmona, J.; Julvez, J.; Cortadella, J.; Kishinevsky, M. **A scheduling strategy for synchronous elastic designs.** *Fundamenta informaticae*. 2011. Volumen: 108. Número: 1-2. Págs.: 1 ~ 21. <<https://doi.org/10.3233/FI-2011-411>>

Julvez, J.; Cortadella, J.; Kishinevsky, M. **On the performance evaluation of multi-guarded marked graphs with single-server semantics.** *Discrete event dynamic systems-theory and applications*. 2010. Volumen: 20. Número: 3. Págs.: 377 ~ 407. <<https://doi.org/10.1007/s10626-009-0079-2>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **New region-based algorithms for deriving bounded Petri nets.** *IEEE transactions on computers*. 2010. Volumen: 59. Número: 3. Págs.: 371 ~ 384. <<https://doi.org/10.1109/TC.2009.131>>

Carmona, J.; Cortadella, J.; Kishinevsky, M.; Taubin, A. **Elastic circuits.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2009. Volumen: 28. Número: 10. Págs.: 1437 ~ 1455. <<https://doi.org/10.1109/TCAD.2009.2030436>>

Cortadella, J.; Taubin, A. **Guest editorial: Special section on asynchronous circuits and systems.** *IEEE transactions on very large scale integration (VLSI) systems*. 2009. Volumen: 17. Número: 7. Págs.: 853 ~ 854. <<https://doi.org/10.1109/TVLSI.2009.2022864>>

Baneres, D.; Cortadella, J.; Kishinevsky, M. **A recursive paradigm to solve boolean relations.** *IEEE transactions on computers*. 2009. Volumen: 58. Número: 4. Págs.: 512 ~ 527. <<https://doi.org/10.1109/TC.2008.165>>

Carmona, J.; Cortadella, J.; Takada, Y.; Peper, F. **Formal methods for the analysis and synthesis of nanometer-scale cellular arrays.** *ACM journal on emerging technologies in computing systems*. 2008. Volumen: 4. Número: 2. Págs.: 8.1 ~ 8.27. <<https://doi.org/10.1145/1350763.1350768>>

Carmona, J.; Cortadella, J. **Encoding large asynchronous controllers with ILP techniques.** *IEEE transactions on computer-aided design of integrated circuits and systems*. 2008. Volumen: 27. Número: 1. Págs.: 20 ~ 33. <<https://doi.org/10.1109/TCAD.2007.907238>>

Cortadella, J.; Kishinevsky, M.; Bufistov, D.; Carmona, J.; Julvez, J. **Elasticity and Petri nets.** *Transactions on petri nets and other models of concurrency*. 2008. Volumen: 1. Págs.: 221 ~ 249. <[https://doi.org/10.1007/978-3-540-89287-8\\_13](https://doi.org/10.1007/978-3-540-89287-8_13)>

Taubin, A.; Cortadella, J.; Lavagno, L.; Kondratyev, A.; Peeters, A. **Design automation of real life asynchronous devices and systems.** *Foundations and trends in electronic design automation*. 2007. Volumen: 2. Número: 1. Págs.: 1 ~ 133. <<https://doi.org/10.1561/1000000006>>

Clarisó, R.; Cortadella, J. **Verification of concurrent systems with parametric delays using octahedra.** *Fundamenta informaticae*. 2007. Volumen: 78. Número: 1. Págs.: 1 ~ 33. <<https://content.iospress.com/articles/fundamenta-informaticae/fi78-1-02>>

Costa, K.; Cortadella, J.; Xia, F.; Yakovlev, A. **Automating synthesis of asynchronous communication mechanisms.** *Fundamenta informaticae*. 2007. Volumen: 78. Número: 1. Págs.: 75 ~ 100. <<https://content.iospress.com/articles/fundamenta-informaticae/fi78-1-04>>

Clarisó, R.; Cortadella, J. **The octahedron abstract domain.** *Science of computer programming*. 2007. Volumen: 64. Número: 1. Págs.: 115 ~ 139. <<https://doi.org/10.1016/j.scico.2006.03.009>>

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Cortadella, J.; Kondratyev, A.; Lavagno, L.; Sotiriou, C. P. **Desynchronization: Synthesis of asynchronous circuits from synchronous specifications.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2006. Volumen: 25. Número: 10. Págs.: 1904 ~ 1921. <<https://doi.org/10.1109/TCAD.2005.860958>>

Carmona, J.; Colom, J.; Cortadella, J.; García-Vallés, F. **Synthesis of asynchronous controllers using integer linear programming.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2006. Volumen: 25. Número: 9. Págs.: 1637 ~ 1651. <<https://doi.org/10.1109/TCAD.2005.859516>>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Passerone, C.; Watanabe, Y. **Quasi-static scheduling of independent tasks for reactive systems.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2005. Volumen: 24. Número: 10. Págs.: 1492 ~ 1514. <<https://doi.org/10.1109/TCAD.2005.852038>>

Clarísó, R.; Rodríguez, E.; Cortadella, J. **Derivation of non-structural invariants of Petri nets using abstract interpretation.** *Lecture notes in computer science.* 2005. Volumen: 3536. Págs.: 188 ~ 207. <[https://doi.org/10.1007/11494744\\_12](https://doi.org/10.1007/11494744_12)>

Clariso, R.; Cortadella, J. **The octahedron abstract domain.** *Lecture notes in computer science.* 2004. Volumen: 3148. Págs.: 312 ~ 327. <[https://doi.org/10.1007/978-3-540-27864-1\\_23](https://doi.org/10.1007/978-3-540-27864-1_23)>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Taubin, A.; Watanabe, Y. **Quasi-static scheduling for concurrent architectures.** *Fundamenta informaticae.* 2004. Volumen: 62. Número: 2. Págs.: 171 ~ 196. <<https://content.iospress.com/articles/fundamenta-informaticae/fi62-2-03>>

Cortadella, J. **Timing-driven logic bi-decomposition.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2003. Volumen: 22. Número: 6. Págs.: 675 ~ 685. <<https://doi.org/10.1109/TCAD.2003.811447>>

Saito, H.; Kondratyev, A.; Cortadella, J.; Lavagno, L.; Nanya, T.; Yakovlev, A. **Design of asynchronous controllers with delay insensitive interface.** *IEICE transactions on fundamentals of electronics, communications and computer sciences.* 2002. Volumen: E85-A. Número: 12. Págs.: 2577 ~ 2585.

Carmona, J.; Cortadella, J. **Input/output compatibility of reactive systems.** *Lecture notes in computer science.* 2002. Volumen: 2517. Págs.: 360 ~ 377. <[https://doi.org/10.1007/3-540-36126-X\\_22](https://doi.org/10.1007/3-540-36126-X_22)>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Passerone, C.; Watanabe, Y. **Quasi-static scheduling of independent tasks for reactive systems.** *Lecture notes in computer science.* 2002. Volumen: 2360. Págs.: 80 ~ 100. <[https://doi.org/10.1007/3-540-48068-4\\_7](https://doi.org/10.1007/3-540-48068-4_7)>

Cortadella, J.; Kishinevsky, M.; Burns, S.; Kondratyev, A.; Lavagno, L.; Stevens, K.; Taubin, A.; Yakovlev, A. **Lazy transition systems and asynchronous circuits synthesis with relative timing assumptions.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 2002. Volumen: 21. Número: 2. Págs.: 109 ~ 130. <<https://doi.org/10.1109/43.980253>>

Carmona, J.; Cortadella, J.; Pastor, E. **A structural encoding technique for the synthesis of asynchronous circuits.** *Fundamenta informaticae.* 2002. Volumen: 50. Número: 2. Págs.: 135 ~ 154. <<https://content.iospress.com/articles/fundamenta-informaticae/fi50-2-03>>

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Pastor, E.; Cortadella, J.; Roig, O. **Symbolic analysis of bounded Petri nets.** *IEEE transactions on computers.* 2001. Volumen: 50. Número: 5. Págs.: 432 ~ 448. <<https://doi.org/10.1109/12.926158>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Hardware and Petri nets: application to asynchronous circuit design.** *Lecture notes in computer science.* 2000. Volumen: 1825. Págs.: 1 ~ 15. <[https://doi.org/10.1007/3-540-44988-4\\_1](https://doi.org/10.1007/3-540-44988-4_1)>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Pastor, E.; Yakovlev, A. **Decomposition and technology mapping of speed-independent circuits using Boolean relations.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 1999. Volumen: 18. Número: 9. Págs.: 1221 ~ 1236. <<https://doi.org/10.1109/43.784116>>

Kondratyev, A.; Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Logic decomposition of speed-independent circuits.** *Proceedings of the IEEE.* 1999. Volumen: 87. Número: 2. Págs.: 347 ~ 362. <<https://doi.org/10.1109/5.740027>>

Sánchez-Carracedo, F.; Cortadella, J.; Badia, R.M. **Optimal exploration of the unrolling degree for software pipelining.** *Journal of systems architecture.* 1999. Volumen: 45. Número: 6-7. Págs.: 505 ~ 517. <[https://doi.org/10.1016/S1383-7621\(98\)00020-4](https://doi.org/10.1016/S1383-7621(98)00020-4)>

Musoll, E.; Lang, T.; Cortadella, J. **Working-zone encoding for reducing the energy in microprocessor address buses.** *IEEE transactions on very large scale integration (VLSI) systems.* 1998. Volumen: 6. Número: 4. Págs.: 568 ~ 572. <<https://doi.org/10.1109/92.736129>>

Pastor, E.; Cortadella, J.; Kondratyev, A.; Roig, O. **Structural methods for the synthesis of speed-independent circuits.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 1998. Volumen: 17. Número: 11. Págs.: 1108 ~ 1129. <<https://doi.org/10.1109/43.736185>>

Musoll, E.; Cortadella, J. **Register-transfer level transformations for low-power data-paths.** *Integrated computer-aided engineering.* 1998. Volumen: 5. Número: 4. Págs.: 315 ~ 332. <<https://doi.org/10.3233/ICA-1998-5403>>

Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Deriving Petri nets from finite transition systems.** *IEEE transactions on computers.* 1998. Volumen: 47. Número: 8. Págs.: 859 ~ 882. <<https://doi.org/10.1109/12.707587>>

Sánchez-Carracedo, F.; Cortadella, J. **Reducing register pressure in software pipelining.** *Journal of information science and engineering.* 1998. Volumen: 14. Número: 1. Págs.: 265 ~ 279. <[http://jise.iis.sinica.edu.tw/JISESearch/pages/View/PaperView.jsf?keyId=102\\_1470](http://jise.iis.sinica.edu.tw/JISESearch/pages/View/PaperView.jsf?keyId=102_1470)>

Kondratyev, A.; Kishinevsky, M.; Taubin, A.; Cortadella, J.; Lavagno, L. **The use of Petri nets for the design and verification of asynchronous circuits and systems.** *Journal of circuits systems and computers.* 1998. Volumen: 8. Número: 1. Págs.: 67 ~ 118. <<https://doi.org/10.1142/S0218126698000055>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **A region-based theory for state assignment in speed-independent circuits.** *IEEE transactions on computer-aided design of integrated circuits and systems.* 1997. Volumen: 16. Número: 8. Págs.: 793 ~ 812. <<https://doi.org/10.1109/43.644602>>

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Lang, T.; Cortadella, J.; Musoll, E. **Individual flip-flops with gated clocks for low power datapaths**. *IEEE transactions on circuits and systems II: analog and digital signal processing*. 1997. Volumen: 44. Número: 6. Págs.: 507 ~ 516. <<https://doi.org/10.1109/82.592586>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers**. *IEICE transactions on information and systems*. 1997. Volumen: E80-D. Número: 3. Págs.: 315 ~ 325. <<http://hdl.handle.net/2117/133565>>

Sánchez-Carracedo, F.; Cortadella, J. **RESIS: a new methodology for register optimization in software pipelining**. *Lecture notes in computer science*. 1996. Volumen: 1124. Págs.: 824 ~ 832. <<https://doi.org/10.1007/BFb0024783>>

Cortadella, J.; Lang, T. **High-radix division and square-root with speculation**. *IEEE transactions on computers*. 1994. Volumen: 43. Número: 8. Págs.: 919 ~ 931. <<https://doi.org/10.1109/12.295854>>

Valero, M.; Cortadella, J.; Gonzalez, A. **Proceedings Euromicro 93: Open System Design: Hardware, Software and Applications: Chairmen's introduction**. *Microprocessing and microprogramming*. 1993. Volumen: 38. Número: 1-5. Págs.: VII. <[https://doi.org/10.1016/0165-6074\(93\)90112-X](https://doi.org/10.1016/0165-6074(93)90112-X)>

Cortadella, J. **Session B2: Processor Architecture II [session introduction]**. *Microprocessing and microprogramming*. 1993. Volumen: 38. Número: 1-5. Págs.: 131 ~ 131. <[https://doi.org/10.1016/0165-6074\(93\)90135-8](https://doi.org/10.1016/0165-6074(93)90135-8)>

Badia, R.M.; Cortadella, J. **Glass: a graph-theoretical approach for global binding**. *Microprocessing and microprogramming*. 1993. Volumen: 38. Número: 1-5. Págs.: 775 ~ 782. <[https://doi.org/10.1016/0165-6074\(93\)90225-A](https://doi.org/10.1016/0165-6074(93)90225-A)>

Sánchez-Carracedo, F.; Cortadella, J. **Resource-constrained pipelining based on loop transformations**. *Microprocessing and microprogramming*. 1993. Volumen: 38. Número: 1-5. Págs.: 429 ~ 436. <[https://doi.org/10.1016/0165-6074\(93\)90178-N](https://doi.org/10.1016/0165-6074(93)90178-N)>

Cortadella, J.; Llaberia, J. **Evaluation of  $A+B=K$  conditions without carry propagation**. *IEEE transactions on computers*. 1992. Volumen: 41. Número: 11. Págs.: 1484 ~ 1488. <<https://doi.org/10.1109/12.177318>>

Cortadella, J.; Jove, T. **Comments on 'Using cache mechanisms to exploit nonrefreshing DRAM's for on-chip memories'**. *IEEE journal of solid-state circuits*. 1992. Volumen: 27. Número: 1. Págs.: 132 ~ 132. <<https://doi.org/10.1109/4.109570>>

Cortadella, J.; Badia, R.M.; Ayguade, E. **Scheduling in a continuous area-time design space**. *Microprocessing and microprogramming*. 1991. Volumen: 32. Número: 1-5. Págs.: 199 ~ 206. <[https://doi.org/10.1016/0165-6074\(91\)90346-U](https://doi.org/10.1016/0165-6074(91)90346-U)>

Cortadella, J.; Llaberia, J. **Making branches transparent to the execution unit**. *International journal of mini and microcomputers*. 1989. Volumen: 11. Número: 1. Págs.: 13 ~ 17.

Jove, T.; Cortadella, J. **Reduced instruction buffer for RISC architectures**. *Microprocessing and microprogramming*. 1989. Volumen: 27. Número: 1. Págs.: 1987 ~ 1993. <[https://doi.org/10.1016/0165-6074\(89\)90026-4](https://doi.org/10.1016/0165-6074(89)90026-4)>

---

Cortadella, J.; Jové, T. **Dynamic RAM for on-chip instruction caches.** *Computer architecture news*. 1988. Volumen: 16. Número: 4. Págs.: 45 ~ 50. <<https://doi.org/10.1145/54331.54336>>

Gonzalez, A.; Llaberia, J.; Cortadella, J. **A mechanism for reducing the cost of branches in RISC architectures.** *Microprocessing and microprogramming*. 1988. Volumen: 24. Número: 1-5. Págs.: 565 ~ 572. <[https://doi.org/10.1016/0165-6074\(88\)90112-3](https://doi.org/10.1016/0165-6074(88)90112-3)>

Cortadella, J.; Jové, T. **Designing a branch target buffer for executing branches with zero time cost in a RISC processor.** *Microprocessing and microprogramming*. 1988. Volumen: 24. Número: 1-5. Págs.: 573 ~ 580. <[https://doi.org/10.1016/0165-6074\(88\)90113-5](https://doi.org/10.1016/0165-6074(88)90113-5)>

Cortadella, J.; Gonzalez, A.; Llaberia, J. **RISC: un nuevo enfoque en el diseño de procesadores.** *Mundo electrónico. Edición internacional*. 1988. Volumen: 1. Número: 180. Págs.: 49 ~ 57.

---

## A.2 Texto en actas de congreso

---

Teren, V.; Cortadella, J.; Villa, T. **Seto: A framework for the decomposition of Petri nets and transition systems.** *2023 26th Euromicro Conference on Digital System Design, DSD 2023: Golem, Durres, Albania, 6-8 September 2023: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2023. Págs.: 669 ~ 677. ISBN/ISSN: 979-8-3503-4419-6. <<https://ieeexplore.ieee.org/xpl/conhome/10456758/proceeding>>

Teren, V.; Cortadella, J.; Villa, T. **Decomposition of transition systems into sets of synchronizing Free-choice Petri Nets.** *2022 25th Euromicro Conference on Digital System Design, DSD 2022: 31 August-2 September 2022, Maspalomas, Spain: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2023. Págs.: 165 ~ 173. ISBN/ISSN: 978-1-6654-7404-7. <<https://ieeexplore.ieee.org/xpl/conhome/9996588/proceeding>>

Castro, J.; Cortadella, J.; Gabarro, J.; Vidal, E. **Programming 1 and Sustainability.** *Towards a new future in engineering education, new scenarios that European alliances of tech universities open up: SEFI 2022: 50th Annual Conference of the European Society for Engineering Education: 19-22 September, Barcelona, Spain: proceedings*. European Society for Engineering Education (SEFI). 2022. Págs.: 1041 ~ 1049. ISBN/ISSN: 978-84-123222-6-2. <<https://www.sefi.be/wp-content/uploads/2022/12/ebook-sefi-2022-1.pdf>>

Teren, V.; Cortadella, J.; Villa, T. **Decomposition of transition systems into sets of synchronizing state machines.** *2021 24th Euromicro Conference on Digital System Design, DSD 2021: virtual conference, 1-3 September 2021: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2021. Págs.: 77 ~ 81. ISBN/ISSN: 978-1-6654-2703-6. <<https://ieeexplore.ieee.org/xpl/conhome/9556315/proceeding>>

Shan, J.; Casu, M.; Cortadella, J.; Lavagno, L.; Lazarescu, M. **Exact and heuristic allocation of multi-kernel applications to multi-FPGA platforms.** *DAC'19: proceedings of the 56th Annual Design Automation Conference 2019, Las Vegas, NV, USA, June 02-06, 2019*. Association for Computing Machinery (ACM). 2019. Págs.: 1 ~ 6. ISBN/ISSN: 978-1-4503-6725-7. <<https://dl.acm.org/citation.cfm?id=3316781>>

Vidal, A.; Cortadella, J.; Petit, J.; Galceran, M.; Martorell, F. **RTL-aware dataflow-driven macro placement.** *Proceedings of the 2019 Design, Automation & Test in Europe (DATE), 25-29 March 2019, Florence, Italy*. Institute of Electrical and Electronics Engineers (IEEE). 2019. Págs.: 186 ~ 191. ISBN/ISSN: 978-3-9819263-2-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8704855>>

Cortadella, J.; Petit, J. **A hierarchical mathematical model for automatic pipelining and allocation using elastic systems.** *Conference record of the Fifty-First Asilomar Conference on Signals, Systems & Computers: October 29-November 1, 2017 Pacific Grove, California*. Institute of Electrical and Electronics Engineers (IEEE).

---

2018. Págs.: 115 ~ 120. ISBN/ISSN: 978-1-5386-1823-3.  
<<http://ieeexplore.ieee.org/servlet/opac?punumber=8330843>>

Moreno, A.; Cortadella, J. **State encoding of asynchronous controllers using pseudo-boolean optimization.** *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems, ASYNC 2018: Vienna, Austria, 13-16 May 2018: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2018. Págs.: 9 ~ 16. ISBN/ISSN: 978-1-5386-5883-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8588203>>

Machado, L.; Roca, A.; Cortadella, J. **Voltage noise analysis with ring oscillator clocks.** *2017 IEEE Computer Society Annual Symposium on VLSI: ISVLSI 2017: 3-5 July 2017, Bochum, North Rhine-Westfalia, Germany: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2017. Págs.: 1 ~ 6. ISBN/ISSN: 978-1-5090-6762-6. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7985547>>

Mokhov, A.; Cortadella, J.; de Gennaro, A. **Process windows.** *17th International Conference on Application of Concurrency to System Design, ACSD 2017: 25-30 June 2017, Zaragoza, Spain: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2017. Págs.: 86 ~ 95. ISBN/ISSN: 978-1-5386-2867-6. <[ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8100276](http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8100276)>

Cortadella, J.; Moreno, A.; Sokolov, D.; Yakovlev, A.; Lloyd, D. **Waveform Transition Graphs: a designer-friendly formalism for asynchronous behaviours.** *23rd International Symposium on Asynchronous Circuits and Systems.* Institute of Electrical and Electronics Engineers (IEEE). 2017. Págs.: 73 ~ 74. ISBN/ISSN: 978-1-5386-2749-5. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8095282>>

Moreno, A.; Cortadella, J. **Synthesis of all-digital delay lines.** *23rd International Symposium on Asynchronous Circuits and Systems.* Institute of Electrical and Electronics Engineers (IEEE). 2017. Págs.: 75 ~ 82. ISBN/ISSN: 978-1-5386-2749-5. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8095282>>

Vidal, A.; Cortadella, J.; Petit, J. **Under-the-cell routing to improve manufacturability.** *Proceedings of the on Great Lakes Symposium on VLSI 2017.* Association for Computing Machinery (ACM). 2017. Págs.: 125 ~ 130. ISBN/ISSN: 978-1-4503-4972-7. <<https://dl.acm.org/citation.cfm?id=3060403&picked=prox>>

Machado, L.; Cortadella, J. **Boolean decomposition for AIG optimization.** *Proceedings of the on Great Lakes Symposium on VLSI 2017.* Association for Computing Machinery (ACM). 2017. Págs.: 143 ~ 148. ISBN/ISSN: 978-1-4503-4972-7. <<https://dl.acm.org/citation.cfm?id=3060403&picked=prox>>

Machado, L.; Roca, A.; Cortadella, J. **Increasing the robustness of digital circuits with ring oscillator clocks.** *2nd International Workshop on Resiliency in Embedded Electronic Systems: SwissTech Convention Centre, Lausanne, Switzerland, March 31st, 2017: final proceedings.* 2017. Págs.: 29 ~ 34. <<http://adt.cs.upb.de/REES2017-Proceedings.pdf>>

San Pedro, J. de; Cortadella, J. **Mining structured Petri nets for the visualization of process behavior.** *Proceedings of the 31st ACM Symposium on Applied Computing.* Association for Computing Machinery (ACM). 2016. Págs.: 839 ~ 846. ISBN/ISSN: 978-145033739-7. <<http://dl.acm.org/citation.cfm?id=2851613&picked=prox&cfid=726075917&cftoken=88385235>>

San Pedro, J. de; Bourgeat, T.; Cortadella, J. **Specification mining for asynchronous controllers.** *22nd IEEE International Symposium on Asynchronous Circuits and Systems: 8-11 May 2016 Porto Alegre, Brazil: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2016. Págs.: 107 ~ 114. ISBN/ISSN: 978-1-4673-9007-1. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7584313>>

---

Cortadella, J.; Lupon, M.; Moreno, A.; Roca, A.; Sapatnekar, S. **Ring oscillator clocks and margins**. *22nd IEEE International Symposium on Asynchronous Circuits and Systems: 8-11 May 2016 Porto Alegre, Brazil: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2016. Págs.: 19 ~ 26. ISBN/ISSN: 978-1-4673-9007-1. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7584313>>

San Pedro, J. de; Cortadella, J. **Discovering duplicate tasks in transition systems for the simplification of process models**. *Business Process Management: 14th International Conference, BPM 2016, Rio de Janeiro, Brazil, September 18-22, 2016: proceedings*. Springer. 2016. Págs.: 108 ~ 124. ISBN/ISSN: 978-3-319-45348-4. <<http://link.springer.com/book/10.1007/978-3-319-45348-4>>

Cortadella, J.; Lavagno, L.; Lopez, P.; Lupon, M.; Moreno, A.; Roca, A.; Sapatnekar, S. **Reactive clocks with variability-tracking jitter**. *Proceedings of the 33rd IEEE International Conference on Computer Design (ICCD): 18-21 October 2015, New York City, USA*. Institute of Electrical and Electronics Engineers (IEEE). 2015. Págs.: 511 ~ 518. ISBN/ISSN: 978-1-4673-7165-0. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7347055>>

San Pedro, J. de; Carmona, J.; Cortadella, J. **Log-based simplification of process models**. *Business Process Management: 13th International Conference, BPM 2015, Innsbruck, Austria, August 31-September 3, 2015: proceedings*. Springer. 2015. Págs.: 457 ~ 474. ISBN/ISSN: 978-3-319-23063-4. <<http://link.springer.com/book/10.1007%2F978-3-319-23063-4>>

Jain, P.; Sapatnekar, S.; Cortadella, J. **A retargetable and accurate methodology for logic-IP-internal electromigration assessment**. *2015 20th Asia and South Pacific Design Automation Conference (ASP-DAC)*. 2015. Págs.: 346 ~ 351. ISBN/ISSN: 978-147997792-5.

San Pedro, J. de; Cortadella, J.; Roca, A. **A hierarchical approach for generating regular floorplans**. *2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD): digest of technical papers: November 2-6, 2014: Hilton San Jose Hotel, San Jose, CA*. Institute of Electrical and Electronics Engineers (IEEE). 2014. Págs.: 655 ~ 662. ISBN/ISSN: 978-1-4799-6277-8. <<http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6991350>>

Beer, S.; Cannizzaro, M.; Cortadella, J.; Ginosar, R.; Lavagno, L. **Metastability in better-than-worst-case designs**. *20th IEEE International Symposium on Asynchronous Circuits and Systems: 12-14 May 2014, Potsdam, Germany: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2014. Págs.: 101 ~ 102. ISBN/ISSN: 978-147993789-9.

Dimitrakopoulos, G.; Seitanidis, I.; Psarras, A.; Tsiouris, K.; Mattheakis, P.; Cortadella, J. **Hardware primitives for the synthesis of multithreaded elastic systems**. *Design, Automation and Test in Europe: proceedings: Dresden, Germany: March 24-28, 2014*. European Interactive Digital Advertising Alliance (EDAA). 2014. Págs.: 1 ~ 4. ISBN/ISSN: 978-398153702-4.

San Pedro, J. de; Nikitin, N.; Cortadella, J.; Petit, J. **Physical planning for the architectural exploration of large-scale chip multiprocessors**. *2013 Seventh IEEE/ACM International Symposium on Networks on Chip (NoCS)*. 2013. Págs.: 1 ~ 2. ISBN/ISSN: 978-1-4673-6491-1.

Cortadella, J.; San Pedro, J. de; Nikitin, N.; Petit, J. **Physical-aware system-level design for tiled hierarchical chip multiprocessors**. *ISPD '13: Proceedings of the 2013 ACM International Symposium on Physical Design: March 24-27, 2013, Stateline, Nevada*. Association for Computing Machinery (ACM). 2013. Págs.: 3 ~ 10. ISBN/ISSN: 978-1-4503-1867-9. <<http://dl.acm.org/citation.cfm?id=2451916&picked=prox&cfid=364452153&cftoken=56650864>>

---

Nikitin, N.; San Pedro, J. de; Carmona, J.; Cortadella, J. **Analytical performance modeling of hierarchical interconnect fabrics**. *Proceedings of the 2012 Sixth IEEE/ACM International Symposium on Networks-on-Chip: 9-11 May 2012, Copenhagen, Denmark*. Institute of Electrical and Electronics Engineers (IEEE). 2012. Págs.: 107 ~ 114. ISBN/ISSN: 978-0-7695-4677-3.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6209063>>

San Pedro, J. de; Carmona, J.; Cortadella, J.; Petit, J. **Integrating formal verification in an online judge for e-Learning logic circuit design**. *SIGCSE '12: proceedings of the 43rd ACM Technical Symposium on Computer Science Education: Raleigh, North Carolina, USA, February 29-March 03, 2012*. Association for Computing Machinery (ACM). 2012. Págs.: 451 ~ 456. ISBN/ISSN: 978-1-4503-1098-7.  
<<https://dl.acm.org/citation.cfm?id=2157136>>

Nikitin, N.; Cortadella, J. **Static task mapping for tiled chip multiprocessors with multiple voltage islands**. *Architecture of Computing Systems – ARCS 2012. 25th International Conference. Munich, Germany, February 28 – March 2, 2012 Proceedings*. Springer. 2012. Págs.: 50 ~ 62. ISBN/ISSN: 978-3-642-28293-5.  
<<http://link.springer.com/book/10.1007/978-3-642-28293-5>>

Perez, J.; Moll, F.; Cortadella, J. **Measuring the tolerance of self-adaptive clocks to supply voltage noise**. *26th Conference on Design of Circuits and Integrated Systems : the next 25 years*. 2011. Págs.: 399 ~ 404.

Galceran, M.; Cortadella, J.; Bufistov, D.; Kishinevsky, M. **Automatic microarchitectural pipelining**. *Design, Automation & Test in Europe: Dresden, Germany, March 8-12, 2010: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2010. Págs.: 961 ~ 964. ISBN/ISSN: 978-3-9810801-6-2.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5450668>>

Nikitin, N.; Chatterjee, S.; Cortadella, J.; Kishinevsky, M.; Ogras, U. **Physical-aware link allocation and route assignment for chip multiprocessing**. *The Fourth ACM/IEEE International Symposium on Networks-on-Chip, NOCS 2010: 3-6 May 2010, Grenoble, France: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2010. Págs.: 125 ~ 134. ISBN/ISSN: 978-0-7695-4053-5.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5476379>>

Cortadella, J.; Lavagno, L.; Amiri, D.; Casanova, J.; Macián, C.; Martorell, F.; Moya, J.; Necchi, L.; Sokolov, D.; Tuncer, E. **Narrowing the margins with elastic clocks**. *2010 IEEE International Conference on Integrated Circuit Design and Technology, ICICDT: MINATEC, Grenoble, France, June 2-June 4, 2010*. Institute of Electrical and Electronics Engineers (IEEE). 2010. Págs.: 146 ~ 150. ISBN/ISSN: 978-1-4244-5775-5.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5506322>>

Cortadella, J.; Galceran, M.; Kishinevsky, M. **Elastic systems**. *Eighth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2010)*. Institute of Electrical and Electronics Engineers (IEEE). 2010. Págs.: 149 ~ 158. ISBN/ISSN: 978-1-4244-7886-6.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5550962>>

Carmona, J.; Cortadella, J. **Process mining meets abstract interpretation**. *Machine Learning and Knowledge Discovery in Databases European Conference, ECML PKDD 2010: Barcelona, Spain, September 20-24, 2010: proceedings, part I*. Springer. 2010. Págs.: 184 ~ 199. ISBN/ISSN: 978-3-642-15880-3.  
<<https://link.springer.com/book/10.1007/978-3-642-15880-3>>

Galceran, M.; Cortadella, J.; Kishinevsky, M. **Symbolic performance analysis of elastic systems**. *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD): November 7-11, 2010, DoubleTree Hotel San Jose, CA*. Institute of Electrical and Electronics Engineers (IEEE). 2010. Págs.: 778 ~ 785. ISBN/ISSN: 978-1-4244-8192-7. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5638200>>

---

Carmona, J.; Cortadella, J.; Kishinevsky, M. **Divide-and-conquer strategies for process mining**. *Business Process Management: 7th International Conference, BPM 2009: Ulm, Germany, September 8-10, 2009: Proceedings (LNCS; 5701)*. Springer. 2009. Págs.: 327 ~ 343. ISBN/ISSN: 0302-9743.  
<<http://www.springerlink.com/content/ym533731mq2p8m16/>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **Genet: a tool for the synthesis and mining of Petri nets**. *Ninth International Conference on Application of Concurrency to System Design: 1-3 July 2009, Augsburg, Germany: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2009. Págs.: 181 ~ 185. ISBN/ISSN: 978-0-7695-3697-2. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5291028>>

Baneres, D.; Cortadella, J.; Kishinevsky, M. **Variable-latency design by function speculation**. *Design, Automation and Test in Europe: Nice, France, April 20-24, 2009: proceedings*. IEEE Computer Society. 2009. Págs.: 1704 ~ 1709. ISBN/ISSN: 978-1-4244-3781-8.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4926138>>

Baneres, D.; Cortadella, J.; Kishinevsky, M. **Timing-driven N-way decomposition**. *GLSVLSI'09, proceedings of the 19th ACM Great Lakes Symposium on VLSI: Boston Area, MA, USA, May 10-12, 2009*. Association for Computing Machinery (ACM). 2009. Págs.: 363 ~ 368. ISBN/ISSN: 978-1-60558-522-2.  
<<https://dl.acm.org/citation.cfm?id=1531542&picked=prox>>

Tuncer, E.; Cortadella, J.; Lavagno, L. **Enabling adaptability through elastic clocks**. *DAC '09, proceedings of the 46th Annual Design Automation Conference: San Francisco, California, July 26-31, 2009*. Association for Computing Machinery (ACM). 2009. Págs.: 8 ~ 10. ISBN/ISSN: 978-1-60558-497-3.  
<<https://dl.acm.org/citation.cfm?id=1629911&picked=prox>>

Casanova, J.; Cortadella, J. **Multi-level clustering for clock skew optimization**. *Proceedings of the 2009 IEEE/ACM International Conference on Computer-Aided Design: digest of technical papers*. Institute of Electrical and Electronics Engineers (IEEE). 2009. Págs.: 547 ~ 554. ISBN/ISSN: 978-1-60558-800-1.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5357317>>

Nikitin, N.; Cortadella, J. **A performance analytical model for network-on-chip with constant service time routers**. *Proceedings of the 2009 IEEE/ACM International Conference on Computer-Aided Design: digest of technical papers*. Institute of Electrical and Electronics Engineers (IEEE). 2009. Págs.: 571 ~ 578. ISBN/ISSN: 978-1-60558-800-1. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5357317>>

Galceran, M.; Cortadella, J.; Kishinevsky, M. **Speculation in elastic systems**. *DAC '09, proceedings of the 46th Annual Design Automation Conference: San Francisco, California, July 26-31, 2009*. Association for Computing Machinery (ACM). 2009. Págs.: 292 ~ 295. ISBN/ISSN: 978-1-60558-497-3.  
<<https://dl.acm.org/citation.cfm?id=1629911&picked=prox>>

Bufistov, D.; Cortadella, J.; Galceran, M.; Julvez, J.; Kishinevsky, M. **Retiming and recycling for elastic systems with early evaluation**. *DAC '09, proceedings of the 46th Annual Design Automation Conference: San Francisco, California, July 26-31, 2009*. Association for Computing Machinery (ACM). 2009. Págs.: 288 ~ 291. ISBN/ISSN: 978-1-60558-497-3. <<https://dl.acm.org/citation.cfm?id=1629911&picked=prox>>

Carmona, J.; Julvez, J.; Cortadella, J.; Kishinevsky, M. **Scheduling synchronous elastic designs**. *Ninth International Conference on Application of Concurrency to System Design: 1-3 July 2009, Augsburg, Germany: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2009. Págs.: 52 ~ 59. ISBN/ISSN: 978-0-7695-3697-2. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5291028>>

Bufistov, D.; Julvez, J.; Cortadella, J. **Performance optimization of elastic systems using buffer resizing and buffer insertion**. *2008 IEEE/ACM International Conference on Computer-Aided Design: digest of technical*

---

*papers*. Institute of Electrical and Electronics Engineers (IEEE). 2008. Págs.: 442 ~ 448. ISBN/ISSN: 978-1-4244-2819-9. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4670335>>

Kam, T.; Kishinevsky, M.; Cortadella, J.; Galceran, M. **Correct-by-construction microarchitectural pipelining**. *2008 IEEE/ACM International Conference on Computer-Aided Design: digest of technical papers*. Institute of Electrical and Electronics Engineers (IEEE). 2008. Págs.: 434 ~ 441. ISBN/ISSN: 978-1-4244-2819-9. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4670335>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **A region-based algorithm for discovering Petri nets from event logs**. *Business Process Management, 6th International Conference, BPM 2008: Milan, Italy, September 2-4, 2008: proceedings*. Springer. 2008. Págs.: 358 ~ 373. ISBN/ISSN: 978-3-540-85758-7. <<https://link.springer.com/book/10.1007/978-3-540-85758-7>>

Carmona, J.; Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **A symbolic algorithm for the synthesis of bounded Petri nets**. *Applications and Theory of Petri Nets: 29th International Conference, PETRI NETS 2008, Xi'an, China, June 23-27, 2008: proceedings*. Springer. 2008. Págs.: 92 ~ 111. ISBN/ISSN: 978-3-540-68746-7. <<https://link.springer.com/book/10.1007/978-3-540-68746-7>>

Gorgônio, K.; Cortadella, J. **Hardware synthesis for asynchronous communications mechanisms**. *International Conference of the Chilean Computer Science Society, SCCC 2008: 10-14 November 2008, Punta Arenas, Chile: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2008. Págs.: 135 ~ 143. ISBN/ISSN: 978-0-7695-3403-9. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4685747>>

Cortadella, J.; Kishinevsky, M. **Synchronous elastic circuits with early evaluation and token counterflow**. *DAC '07: Proceedings of the 44th Annual Design Automation Conference: San Diego, California, June 04-08, 2007*. Association for Computing Machinery (ACM). 2007. Págs.: 416 ~ 419. ISBN/ISSN: 978-1-59593-627-1. <<https://dl.acm.org/citation.cfm?id=1278480&picked=prox>>

Bañeres, D.; Cortadella, J.; Kishinevsky, M. **Layout-aware gate duplication and buffer insertion**. *2007 Design, Automation and Test in Europe Conference and Exposition, DATE 2007: Nice, France, April 16-20, 2007*. Association for Computing Machinery (ACM). 2007. Págs.: 1367 ~ 1372. ISBN/ISSN: 978-3-9810801-2-4. <<https://dl.acm.org/citation.cfm?id=1266366&picked=prox>>

Bufistov, D.; Cortadella, J.; Kishinevsky, M.; Sapatnekar, S. **A general model for performance optimization of sequential systems**. *2007 International Conference on Computer-Aided Design, ICCAD 2007: San Jose, CA, USA, November 5-8, 2007*. Institute of Electrical and Electronics Engineers (IEEE). 2007. Págs.: 362 ~ 369. ISBN/ISSN: 978-1-4244-1381-2. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4397222>>

Carmona, J.; Cortadella, J.; Takada, Y.; Peper, F. **From molecular interactions to gates: a systematic approach**. *ICCAD '06: Proceedings of the 2006 IEEE/ACM International conference on Computer-Aided Design: San Jose, California, November 05-09, 2006*. Association for Computing Machinery (ACM). 2006. Págs.: 891 ~ 898. ISBN/ISSN: 1-59593-389-1. <<https://dl.acm.org/citation.cfm?doid=1233501.1233590>>

Krstic, S.; Cortadella, J.; Kishinevsky, M.; O'Leary, J. **Synchronous elastic networks**. *Proceedings of Formal Methods in Computer Aided Design: 12-16 November 2006, San Jose, California, USA*. Institute of Electrical and Electronics Engineers (IEEE). 2006. Págs.: 19 ~ 30. ISBN/ISSN: 978-0-7695-2707-9. <<https://ieeexplore.ieee.org/document/4021004>>

Julvez, J.; Cortadella, J.; Kishinevsky, M. **Performance analysis of concurrent systems with early evaluation**. *ICCAD '06: Proceedings of the 2006 IEEE/ACM International conference on Computer-Aided Design: San Jose,*

---

California, November 05-09, 2006. Association for Computing Machinery (ACM). 2006. Págs.: 448 ~ 455. ISBN/ISSN: 1-59593-389-1. <<https://dl.acm.org/citation.cfm?doid=1233501.1233590>>

Carmona, J.; Cortadella, J. **State encoding of large asynchronous controllers**. *Design Automation Conference, 43rd DAC: The Moscone Center, San Francisco, CA, July 24-28, 2006: proceedings 2006*. Association for Computing Machinery (ACM). 2006. Págs.: 939 ~ 944. ISBN/ISSN: 1-59593-381-6. <<https://dl.acm.org/citation.cfm?id=1146909&picked=prox>>

Cortadella, J.; Kishinevsky, M.; Grundmann, B. **Synthesis of synchronous elastic architectures**. *Design Automation Conference, 43rd DAC: The Moscone Center, San Francisco, CA, July 24-28, 2006: proceedings 2006*. Association for Computing Machinery (ACM). 2006. Págs.: 657 ~ 662. ISBN/ISSN: 1-59593-381-6. <<https://dl.acm.org/citation.cfm?id=1146909&picked=prox>>

Bañeres, D.; Cortadella, J.; Kishinevsky, M. **Dominator-based partitioning for delay optimization**. *GLSVLSI '06: proceedings of the 16th ACM Great Lakes Symposium on VLSI: Philadelphia, PA, USA, April 30-May 01, 2006*. Association for Computing Machinery (ACM). 2006. Págs.: 67 ~ 72. ISBN/ISSN: 1-59593-347-6. <<https://dl.acm.org/citation.cfm?id=1127908&picked=prox>>

Cortadella, J.; Kishinevsky, M.; Grundmann, B. **SELF: Specification and design of synchronous elastic circuits**. *Proceedings ACM/IEEE International Workshop on Timing Issues*. Vinod Kariat. 2006. Págs.: 16 ~ 21.

Sánchez-Carracedo, F.; Cortadella, J. **Time-constrained loop pipelining**. *Proceedings of the 1995 IEEE/ACM International Conference on Computer-Aided Design, ICCAD 1995: San Jose, California, USA, November 5-9, 1995*. Institute of Electrical and Electronics Engineers (IEEE). 2005. Págs.: 592 ~ 596. ISBN/ISSN: 0-8186-7213-7. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3472>>

Cortadella, J.; Costa, K.; Xia, F.; Yakovlev, A. **Automating synthesis of asynchronous communication mechanisms**. *Fifth International Conference on Application of Concurrency to System Design, ACSD 2005: 7-9 June 2005, St. Malo, France: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2005. Págs.: 166 ~ 175. ISBN/ISSN: 0-7695-2363-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=10077>>

Clarísó, R.; Cortadella, J. **Verification of concurrent systems with parametric delays using octahedra**. *Fifth International Conference on Application of Concurrency to System Design, ACSD 2005: 7-9 June 2005, St. Malo, France: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2005. Págs.: 122 ~ 131. ISBN/ISSN: 0-7695-2363-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=10077>>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Sotiriou, C. P. **Coping with the variability of combinational logic delays**. *IEEE International Conference on Computer Design: VLSI in Computers & Processors, ICCD 2004: 11-13 October 2004, San Jose, CA: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2004. Págs.: 505 ~ 508. ISBN/ISSN: 0-7695-2231-9. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=9333>>

Bañeres, D.; Cortadella, J.; Kishinevsky, M. **A recursive paradigm to solve boolean relations**. *Design Automation Conference, 41st DAC: San Diego Convention Center, San Diego, CA, June 7-11, 2004: proceedings 2004*. Association for Computing Machinery (ACM). 2004. Págs.: 416 ~ 421. ISBN/ISSN: 1-58113-828-8. <<https://dl.acm.org/citation.cfm?id=996566&picked=prox>>

Blunno, I.; Cortadella, J.; Kondratyev, A.; Lavagno, L.; Lwin, K.; Sotiriou, C. P. **Handshake protocols for de-synchronization**. *10th IEEE International Symposium on Asynchronous Circuits and Systems, ASYNC 2004: 19-23 April 2004, Crete, Greece*. Institute of Electrical and Electronics Engineers (IEEE). 2004. Págs.: 149 ~ 158. ISBN/ISSN: 0-7695-2133-9. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=9094>>

---

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Lwin, K.; Sotiriou, C. P. **From synchronous to asynchronous: an automatic approach.** *Design, Automation and Test in Europe Conference and Exhibition: Paris, France, February 16–20, 2004.* Institute of Electrical and Electronics Engineers (IEEE). 2004. Págs.: 1368 ~ 1369. ISBN/ISSN: 0-7695-2085-5. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8959>>

Modi, N.; Cortadella, J. **Boolean decomposition using two-literal divisors.** *17th International Conference on VLSI Design: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2004. Págs.: 765 ~ 768. ISBN/ISSN: 0-7695-2072-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8911>>

Clarísó, R.; Cortadella, J. **Verification of parametric timed circuits using octahedra.** *Fifth International Workshop on Designing Correct Circuits: Barcelona, 27-28 March 2004: a satellite event of the ETAPS 2004 group of conferences: participants' proceedings.* 2004.

Clarísó, R.; Cortadella, J. **Verification of timed circuits with symbolic delays.** *Proceedings of the ASP-DAC 2004 Asia and South Pacific Design Automation Conference 2004: January 27-January 30, 2004, Pacifico Yokohama, Yokohama, Japan.* Institute of Electrical and Electronics Engineers (IEEE). 2004. Págs.: 628 ~ 633. ISBN/ISSN: 0-7803-8175-0. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=9284>>

Clarísó, R.; Cortadella, J. **The octahedron abstract domain.** *Static Analysis: 11th International Symposium, SAS 2004: Verona, Italy, August 26-28, 2004: proceedings.* Springer. 2004. Págs.: 312 ~ 327. ISBN/ISSN: 978-3-540-27864-1. <<http://link.springer.com/book/10.1007/b99688>>

Carmona, J.; Cortadella, J. **ILP models for the synthesis of asynchronous control circuits.** *ICCAD-2003, International Conference on Computer Aided Design: November 9-13, 2003, DoubleTree Hotel, San Jose, CA.* Association for Computing Machinery (ACM). 2003. Págs.: 818 ~ 825. ISBN/ISSN: 1-58113-762-1. <<https://dl.acm.org/citation.cfm?id=1009982>>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Watanabe, Y. **Quasi-static scheduling for concurrent architectures.** *Third International Conference on Application of Concurrency to System Design, ACS2003: 18-20 June 2003, Guimarães, Portugal: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2003. Págs.: 29 ~ 40. ISBN/ISSN: 0-7695-1887-7. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8583>>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Sotiriou, C. P. **A concurrent model for de-synchronization.** *International Workshop on Logic and Synthesis.* Diana Marculescu and Yuji Kukimoto. 2003. Págs.: 294 ~ 302.

Clarísó, R.; Cortadella, J. **Verification of timed circuits with symbolic delays.** *International Workshop on Logic and Synthesis.* Diana Marculescu and Yuji Kukimoto. 2003. Págs.: 310 ~ 317.

Carmona, J.; Cortadella, J. **Input/output compatibility of reactive systems.** *Formal Methods in Computer-Aided Design, 4th International Conference, FMCAD 2002: Portland, OR, USA, November 6-8, 2002: proceedings.* Springer. 2002. Págs.: 360 ~ 377. ISBN/ISSN: 978-3-540-36126-8. <<https://link.springer.com/book/10.1007/3-540-36126-X>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Hazard-free logic synthesis and technology mapping.** *Summer School on Asynchronous Circuit Design: lecture notes: July 15-19, 2002, TIMA Laboratory, Grenoble-France.* 2002. Págs.: 1 ~ 27.

Cortadella, J.; Yakovlev, A. **Petrify.** *Summer School on Asynchronous Circuit Design: lecture notes: July 15-19, 2002, TIMA Laboratory, Grenoble-France.* 2002. Págs.: 1 ~ 30.

---

Cortadella, J. **Bi-decomposition and tree-height reduction for timing optimization.** *IWLS-02, 11th IEEE/ACM International Workshop on Logic & Synthesis: June 4-7, 2002, New Orleans, Louisiana, USA.* Institute of Electrical and Electronics Engineers (IEEE). 2002. Págs.: 233 ~ 238.

Clariso, R.; Cortadella, J.; Kondratyev, A.; Lavagno, L.; Passerone, C.; Watanabe, Y. **Synthesis of embedded software for reactive systems.** *Integration of Software Specification Techniques: Workshop, INT'02 [held as part of the joint European Conferences on Theory and Practice of Software]; ETAPS 2002, Grenoble, France, april 6-14, 2002.* 2002. Págs.: 2 ~ 20.

Peña, M.; Cortadella, J.; Pastor, E.; Smirnov, A. **A case study for the verification of complex timed circuits: IPCMOS.** *2002 Design, Automation and Test in Europe Conference and Exhibition: March 4-8, 2002, Paris, France: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2002. Págs.: 44 ~ 51. ISBN/ISSN: 0-7695-1471-5. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7834>>

Cortadella, J.; Yakovlev, A.; Garside, J. **Logic design of asynchronous circuits.** *7th Asia and South Pacific Design Automation Conference; 15th International Conference on VLSI Design: 7-11 January 2002, Bangalore, India: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2002. Págs.: 26 ~ 27. ISBN/ISSN: 0-7695-1441-3. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7806>>

Cornetta, G.; Cortadella, J. **Asynchronous multipliers with variable-delay counters.** *ICECS 2001, The 8th IEEE International Conference on Electronics, Circuits and Systems: September 2nd-5th, 2001, Malta.* Institute of Electrical and Electronics Engineers (IEEE). 2001. Págs.: 701 ~ 705. ISBN/ISSN: 0-7803-7057-0. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7591>>

Carmona, J.; Cortadella, J.; Pastor, E. **A structural encoding technique for the synthesis of asynchronous circuits.** *Second International Conference on Application of Concurrency to System Design, 25-29 June 2001, Newcastle upon Tyne, UK: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2001. Págs.: 157 ~ 166. ISBN/ISSN: 0-7695-1071-X. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7716>>

Cornetta, G.; Cortadella, J. **A multi-radix approach to asynchronous division.** *Seventh International Symposium on Asynchronous Circuits and Systems, ASYNC 2001: March 11-14, 2001, Salt Lake City, Utah: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2001. Págs.: 25 ~ 34. ISBN/ISSN: 0-7695-1034-5. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7299>>

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Massot, M.; Moral, S.; Passerone, C.; Watanabe, Y.; Sangiovanni-Vincentelli, A. **Task generation and compile-time scheduling for mixed data-control embedded software.** *37th Design Automation Conference: Los Angeles Convention Center, Los Angeles, CA, June 5-9, 2000: proceedings.* Association for Computing Machinery (ACM). 2000. Págs.: 489 ~ 494. ISBN/ISSN: 1-58113-352-9.

Peña, M.; Cortadella, J.; Kondratyev, A.; Pastor, E. **Formal verification of safety properties in timed circuits.** *Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2000): April 2-6, 2000, Eilat, Israel: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 2000. Págs.: 2 ~ 11. ISBN/ISSN: 0-7695-0586-4. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6759>>

Cortadella, J.; Valiente, G. **A relational view of subgraph isomorphism.** *ReMiCS 2000: 5th International Seminar on Relational Methods in Computer Science.* Université Laval. 2000. Págs.: 45 ~ 54.

Cortadella, J.; Kishinevsky, M.; Burns, S.; Stevens, K. **Synthesis of asynchronous control circuits with automatically generated relative timing assumptions.** *1999 IEEE/ACM International Conference on Computer-Aided Design: November 7-11, 1999, San Jose, California: digest of technical papers.* Institute of Electrical and

---

Electronics Engineers (IEEE). 1999. Págs.: 324 ~ 331. ISBN/ISSN: 0-7803-5832-5.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6570>>

Saito, H.; Kondratyev, A.; Cortadella, J.; Lavagno, L.; Yakovlev, A. **What is the cost of delay insensitivity?** 1999 *IEEE/ACM International Conference on Computer-Aided Design: November 7-11, 1999, San Jose, California: digest of technical papers*. Institute of Electrical and Electronics Engineers (IEEE). 1999. Págs.: 316 ~ 323. ISBN/ISSN: 0-7803-5832-5. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6570>>

Kondratyev, A.; Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Automatic synthesis and optimization of partially specified asynchronous systems.** *36th Design Automation Conference: Ernest N. Morial Convention Center, New Orleans, LA, June 21-25, 1999: proceedings*. Association for Computing Machinery (ACM). 1999. Págs.: 110 ~ 115. ISBN/ISSN: 1-58113-092-9. <<https://dl.acm.org/citation.cfm?id=309893>>

Stevens, K.; Rotem, S.; Burns, S.; Cortadella, J.; Ginosar, R.; Kishinevsky, M.; Roncken, M. **CAD directions for high performance asynchronous circuits.** *36th Design Automation Conference: Ernest N. Morial Convention Center, New Orleans, LA, June 21-25, 1999: proceedings*. Association for Computing Machinery (ACM). 1999. Págs.: 116 ~ 121. ISBN/ISSN: 1-58113-092-9. <<https://dl.acm.org/citation.cfm?id=309893>>

Pastor, E.; Cortadella, J.; Peña, M. **Structural methods to improve the symbolic analysis of Petri nets.** *Application and Theory of Petri Nets 1999, 20th International Conference, ICATPN'99: Williamsburg, Virginia, USA, June 21-25, 1999: proceedings*. Springer. 1999. Págs.: 26 ~ 45. ISBN/ISSN: 978-3-540-48745-6.  
<<https://link.springer.com/book/10.1007/3-540-48745-X>>

Taubin, A.; Kondratyev, A.; Cortadella, J.; Lavagno, L. **Behavioral transformations to increase the noise immunity of asynchronous specifications.** *Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems: April 19-21, 1999, Barcelona, Spain: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1999. Págs.: 36 ~ 47. ISBN/ISSN: 0-7695-0031-5.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6163>>

Cornetta, G.; Cortadella, J. **A radix-16 SRT division unit with speculation of the quotient digits.** *Ninth Great Lakes Symposium on VLSI: Ypsilanti Marriott at Eagle Court, Ypsilanti, Michigan, March 4-6, 1999: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1999. Págs.: 74 ~ 77. ISBN/ISSN: 0-7695-0104-4.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6127>>

Taubin, A.; Kondratyev, A.; Cortadella, J.; Lavagno, L. **Crosstalk noise avoidance in asynchronous circuits.** *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*. ACM/IEEE. 1999. Págs.: 123 ~ 128.

Saito, H.; Kondratyev, A.; Cortadella, J.; Lavagno, L.; Yakovlev, A. **Bridging modularity and optimality: delay-insensitive interfacing in asynchronous circuits synthesis.** *IEEE SMC'99 conference proceedings: 1999 IEEE International Conference on Systems, Man, and Cybernetics: October 12-15, 1999, Tokyo, Japan*. Institute of Electrical and Electronics Engineers (IEEE). 1999. Págs.: 899 ~ 904. ISBN/ISSN: 0-7803-5731-0.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6569>>

Peña, M.; Pastor, E.; Cortadella, J. **A symbolic technique for the efficient ATPG of speed-independent circuits.** *Proceedings of the XIV Design of Circuits and Integrated Systems Conference: Palma de Mallorca, Spain, november 16-19, 1999*. Universitat de les Illes Balears. 1999. Págs.: 295 ~ 300. ISBN/ISSN: 84-7632-424-3.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Taubin, A.; Yakovlev, A. **Lazy transition systems: application to timing optimization of asynchronous circuits.** *1998 International Conference on Computer-Aided Design: November 8-12, 1998, San Jose, California: digest of technical papers*. Institute of Electrical and

---

Electronics Engineers (IEEE). 1998. Págs.: 324 ~ 331. ISBN/ISSN: 1-58113-008-2.  
<<https://dl.acm.org/citation.cfm?id=288633>>

Lang, T.; Mussol, E.; Cortadella, J. **Extension of the working-zone-encoding method to reduce the energy on the microprocessor data bus.** *International Conference on Computer Design: VLSI in Computers and Processors: October 5-7, 1998 Austin, Texas: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1998. Págs.: 414 ~ 419. ISBN/ISSN: 0-8186-9099-2.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5873>>

Pastor, E.; Cortadella, J. **Structural methods applied to the symbolic analysis of Petri nets.** *IWLS'98 International Workshop on Logic Synthesis.* Fabio Somenzi. 1998. Págs.: 276 ~ 283.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Automatic handshake expansion and reshuffling using concurrency reduction.** *HWPN'98, Workshop on Hardware Design and Petri Nets: June 23, 1998, Hotel Costa da Caparica, Lisbon, Portugal.* 1998. Págs.: 86 ~ 110.

Cortadella, J. **Asynchronous circuit verification and synthesis with Petri nets.** *HWPN'98, Workshop on Hardware Design and Petri Nets: June 23, 1998, Hotel Costa da Caparica, Lisbon, Portugal.* 1998. Págs.: 1 ~ 11.

Mussol, E.; Lang, T.; Cortadella, J. **Reducing the energy of address and data buses with the working-zone encoding technique and its effect on multimedia applications.** *Power Driven Microarchitecture Workshop: in conjunction with ISCA 98, Barcelona, Spain, Sunday, June 28, 1998.* 1998. Págs.: 3 ~ 8.

Kishinevsky, M.; Cortadella, J.; Kondratyev, A. **Asynchronous interface specification, analysis and synthesis.** *DAC '98: Proceedings of the 35th annual Design Automation Conference: San Francisco, California, USA, June 15-19, 1998.* Association for Computing Machinery (ACM). 1998. Págs.: 2 ~ 7. ISBN/ISSN: 0-89791-964-5.  
<<https://dl.acm.org/citation.cfm?id=277044&picked=prox>>

Cortadella, J. **Combining structural and symbolic methods for the verification of concurrent systems.** *1998 International Conference on Application of Concurrency to System Design: March 23-26, 1998, Fukushima, Japan: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1998. Págs.: 2 ~ 7. ISBN/ISSN: 0-8186-8350-3. <<https://ieeexplore.ieee.org/recursos/xpl/mostRecentIssue.jsp?punumber=5285>>

Kondratyev, A.; Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Taubin, A.; Yakovlev, A. **Identifying state coding conflicts in asynchronous system specifications using Petri net unfoldings.** *1998 International Conference on Application of Concurrency to System Design: March 23-26, 1998, Fukushima, Japan: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1998. Págs.: 152 ~ 163. ISBN/ISSN: 0-8 186-8350-3.  
<<https://ieeexplore.ieee.org/recursos/xpl/mostRecentIssue.jsp?punumber=5285>>

Pastor, E.; Cortadella, J. **Efficient encoding schemes for symbolic analysis of Petri nets.** *Design, Automation and Test in Europe: February 23-26, 1998 Paris, France: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1998. Págs.: 790 ~ 795. ISBN/ISSN: 0-8186-8359-7.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5270>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Pastor, E.; Yakovlev, A. **Decomposition and technology mapping of speed-independent circuits using Boolean relations.** *1997 IEEE/ACM International Conference on Computer-Aided Design: November 9-13, 1997 San Jose, California.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 220 ~ 227. ISBN/ISSN: 0-8186-8200-0.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5191>>

---

Musoll, E.; Lang, T.; Cortadella, J. **Exploiting the locality of memory references to reduce the address bus energy.** *1997 International Symposium on Low Power Electronics and Design: Doubletree Hotel, Monterey, CA, August 18-20, 1997: proceedings.* Association for Computing Machinery (ACM). 1997. Págs.: 202 ~ 207. ISBN/ISSN: 0-89791-903-3. <<https://dl.acm.org/citation.cfm?id=263272>>

Semenov, A.; Yakovlev, A.; Pastor, E.; Peña, M.; Cortadella, J. **Synthesis of speed-independent circuits from STG-unfolding segment.** *Design Automation Conference, 34th DAC: Anaheim, CA, Anaheim Convention Center, June 9-13, 1997: proceedings 1997.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 16 ~ 21. ISBN/ISSN: 0-7803-4093-0. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4655>>

Roig, O.; Cortadella, J.; Peña, M.; Pastor, E. **Automatic generation of synchronous test patterns for asynchronous circuits.** *Design Automation Conference, 34th DAC: Anaheim, CA, Anaheim Convention Center, June 9-13, 1997: proceedings 1997.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 620 ~ 625. ISBN/ISSN: 0-7803-4093-0. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4655>>

Kondratyev, A.; Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Technology mapping for speed-independent circuits: Decomposition and resynthesis.** *Third International Symposium on Advanced Research in Asynchronous Circuits and Systems: April 7-10, 1997, Eindhoven, The Netherlands: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 240 ~ 253. ISBN/ISSN: 0-8186-7922-0.

Semenov, A.; Yakovlev, A.; Pastor, E.; Peña, M.; Cortadella, J.; Lavagno, L. **Partial order based approach to synthesis of speed-independent circuits.** *Third International Symposium on Advanced Research in Asynchronous Circuits and Systems: April 7-10, 1997, Eindhoven, The Netherlands: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 254 ~ 265. ISBN/ISSN: 0-8186-7922-0.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Technology mapping of speed-independent circuits based on combinational decomposition and resynthesis.** *European Design and Test Conference, ED&TC 97: March 17-20, 1997, Paris, France: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1997. Págs.: 98 ~ 105. ISBN/ISSN: 0-8186-7786-4. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4452>>

Lang, T.; Musoll, E.; Cortadella, J. **Redundant adder for reduced output transitions.** *DCIS96, XI Design of Integrated Circuits and Systems Conference: proceedings.* Universitat Politècnica de Catalunya. 1996. Págs.: 17 ~ 22. ISBN/ISSN: 84-89349-83-5.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers.** *DCIS96, XI Design of Integrated Circuits and Systems Conference: proceedings.* Universitat Politècnica de Catalunya. 1996. Págs.: 205 ~ 210. ISBN/ISSN: 84-89349-83-5.

Cortadella, J.; Badia, R.M.; Sánchez-Carracedo, F. **A mathematical formulation of the loop pipelining problem.** *DCIS96, XI Design of Integrated Circuits and Systems Conference: proceedings.* Universitat Politècnica de Catalunya. 1996. Págs.: 355 ~ 360. ISBN/ISSN: 84-89349-83-5.

Sintes, L.; Escudero, J.; Peña, M.; Roig, O.; Cortadella, J.; Carrabina, J. **Flujo de diseño asíncrono con la biblioteca DCVSL\_LIB para ES2 ECPD10.** *II Congreso sobre Tecnologías Aplicadas a la Enseñanza de la Electrónica: Sevilla, 19 y 20 de septiembre de 1996.* Omron. 1996. Págs.: 161 ~ 166.

Sánchez-Carracedo, F.; Cortadella, J. **RESIS: A new methodology for register optimization in software pipelining.** *Euro-Par'96, Parallel Processing: Second International Euro-Par Conference: Lyon, France, August*

---

26–29, 1996: *proceedings, volume II*. Springer. 1996. Págs.: 824 ~ 832. ISBN/ISSN: 978-3-540-70636-6.  
<<https://link.springer.com/book/10.1007/BFb0024677>>

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Methodology and tools for state encoding in asynchronous circuit synthesis**. *Proceedings 1996: 33rd Design Automation Conference, Las Vegas Convention Center, Las Vegas, NV, June 3-7, 1996*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 63 ~ 66. ISBN/ISSN: 0-7803-3294-6.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3826>>

Sánchez-Carracedo, F.; Cortadella, J. **Maximum-throughput software pipelining**. *Proceedings of the Second International Conference on Massively Parallel Computing Systems: May 6-9, 1996, Ischia, Italy*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 464 ~ 473. ISBN/ISSN: 0818676000.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Complete state encoding based on the theory of regions**. *Second International Symposium on Advanced Research in Asynchronous Circuits and Systems: March 18-21, 1996 Aizu-Wakamatsu, Fukushima, Japan: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 36 ~ 47. ISBN/ISSN: 0-8186-7298-6.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3564>>

Peña, M.; Cortadella, J. **Combining process algebras and Petri nets for the specification and synthesis of asynchronous circuits**. *Second International Symposium on Advanced Research in Asynchronous Circuits and Systems: March 18-21, 1996 Aizu-Wakamatsu, Fukushima, Japan: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 222 ~ 232. ISBN/ISSN: 0-8186-7298-6.  
<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3564>>

Musoll, E.; Cortadella, J. **Optimizing CMOS circuits for low power using transistor reordering**. *European Design & Test Conference: ED&TC 96: Paris, France: March 11-14, 1996: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 219 ~ 223. ISBN/ISSN: 0-8186-7424-5.  
<<https://ieeexplore.ieee.org/xpl/conhome/3563/proceeding>>

Pastor, E.; Cortadella, J.; Kondratyev, A.; Roig, O. **Structural methods for the synthesis of speed-independent circuits**. *European Design & Test Conference: ED&TC 96: Paris, France: March 11-14, 1996: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 1996. Págs.: 340 ~ 347. ISBN/ISSN: 0-8186-7424-5.  
<<https://ieeexplore.ieee.org/xpl/conhome/3563/proceeding>>

Pastor, E.; Cortadella, J.; Kondratyev, A.; Roig, O. **Cover approximations for the synthesis of speed-independent circuits**. *Proceedings: International Workshop on Logic and Architecture Synthesis, December 18-19, 1995*. Institut National Polytechnique de Grenoble. 1995. Págs.: 150 ~ 159.

Peña, M.; Cortadella, J. **Programación VLSI y síntesis de circuitos asíncronos mediante composición de redes de Petri**. *X Congreso de Diseño de Circuitos Integrados y Sistemas: DCIS/SICD'95: Zaragoza, España: Noviembre, 15-17, 1995: actas*. 1995. Págs.: 65 ~ 70. ISBN/ISSN: 84-600-9269-0.

Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Synthesizing Petri nets from state-based models**. *Proceedings of the 1995 IEEE/ACM International Conference on Computer-Aided Design, ICCAD 1995, San Jose, California, USA, November 5-9, 1995*. Institute of Electrical and Electronics Engineers (IEEE). 1995. Págs.: 164 ~ 171. ISBN/ISSN: 0-8186-7213-7. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3472>>

Musoll, E.; Cortadella, J. **Scheduling and resource binding for low power**. *Proceedings of the Eighth International Symposium on System Synthesis*. Institute of Electrical and Electronics Engineers (IEEE). 1995.

---

Págs.: 104 ~ 109. ISBN/ISSN: 0-8186-7076-2.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4001>>

Roig, O.; Cortadella, J.; Pastor, E. **Verification of asynchronous circuits by BDD-based model checking of Petri nets.** *Application and Theory of Petri Nets 1995, 16th International Conference: Turin, Italy, June 26-30, 1995: proceedings.* Springer. 1995. Págs.: 374 ~ 391. ISBN/ISSN: 978-3-540-49408-9.

<<https://link.springer.com/book/10.1007/3-540-60029-9>>

Roig, O.; Cortadella, J.; Pastor, E. **Hierarchical gate-level verification of speed-independent circuits.** *Second Working Conference on Asynchronous Design Methodologies: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1995. Págs.: 128 ~ 137. ISBN/ISSN: 0-8186-7098-3.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3937>>

Musoll, E.; Cortadella, J. **High-level synthesis techniques for reducing the activity of functional units.** *1995 International Symposium on Low Power Design: proceedings.* Association for Computing Machinery (ACM). 1995. Págs.: 99 ~ 104. ISBN/ISSN: 0-89791-744-8. <<https://dl.acm.org/citation.cfm?id=224081&picked=prox>>

Pastor, E.; Cortadella, J.; Roig, O. **A new look at the conditions for the synthesis of speed-independent circuits.** *Fifth Great Lakes Symposium on VLSI: The State University of New York at Buffalo, March 16-18, 1995: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1995. Págs.: 230 ~ 235. ISBN/ISSN: 0-8186-7035-5. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3883>>

Kondratyev, A.; Cortadella, J.; Kishinevsky, M.; Pastor, E.; Roig, O.; Yakovlev, A. **Checking signal transition graph implementability by symbolic bdd traversal.** *Proceedings the European Design and Test Conference, ED&TC 1995.* Institute of Electrical and Electronics Engineers (IEEE). 1995. Págs.: 325 ~ 332. ISBN/ISSN: 0-8186-7039-8.

Musoll, E.; Cortadella, J. **Low-power array multipliers with transition-retaining barriers.** *PATMOS'95: Power and Timing Modeling for Performance of Integrated Circuits.* 1995. Págs.: 227 ~ 238. ISBN/ISSN: 3-8142-0526-X.

Musoll, E.; Cortadella, J. **Low-power array multipliers with transition-retaining barriers.** *PATMOS'95: Power and Timing Modeling for Performance of Integrated Circuits.* 1995. Págs.: 227 ~ 238. ISBN/ISSN: 3-8142-0526-X.

Sánchez-Carracedo, F.; Cortadella, J. **Resource-constrained software pipelining for high-level synthesis of DSP systems.** *Algorithms an Parallel VLSI architectures III.* Elsevier. 1995. Págs.: 377 ~ 388. ISBN/ISSN: 978-0-444-82106-5. <<https://www.sciencedirect.com/book/9780444821065/algorithms-and-parallel-vlsi-architectures-iii>>

Cortadella, J.; Lavagno, L.; Vanbekbergen, P.; Yakovlev, A. **Designing asynchronous circuits from behavioural specifications with internal conflicts.** *Proceedings of the International Symposium on Advanced Research in Asynchronous Circuits and Systems: November 3-5, 1994, Salt Lake City, Utah.* Institute of Electrical and Electronics Engineers (IEEE). 1994. Págs.: 106 ~ 115. ISBN/ISSN: 0-8186-6210-7.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5265>>

Roig, O.; Pastor, E.; Cortadella, J. **Verificación de circuitos independientes de la velocidad con modelos simbólicos de redes de Petri.** *Actas del IX Congreso de Diseño de Circuitos Integrados: 9, 10 y 11 de noviembre de 1994, Maspalomas, Gran Canaria.* Universidad de las Palmas de Gran Canaria. 1994. Págs.: 307 ~ 312.

Pastor, E.; Cortadella, J. **Polynomial algorithms for the synthesis of hazard-free circuits from signal transition graphs.** *1993 IEEE/ACM International Conference on Computer-Aided Design: November 7-11, 1993, Santa Clara, California: digest of technical papers.* Institute of Electrical and Electronics Engineers (IEEE). 1993.

---

Págs.: 250 ~ 254. ISBN/ISSN: 0-8186-4490-7.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4431>>

Pastor, E.; Cortadella, J. **An efficient unique state coding algorithm for signal transition graphs.** *1993 IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1993. ICCD '93: proceedings.* Institute of Electrical and Electronics Engineers (IEEE). 1993. Págs.: 174 ~ 177. ISBN/ISSN: 0-8186-4230-0.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3140>>

Cortadella, J.; Lang, T. **Division with speculation of quotient digits.** *Proceedings of IEEE 11th Symposium on Computer Arithmetic.* Institute of Electrical and Electronics Engineers (IEEE). 1993. Págs.: 87 ~ 94. ISBN/ISSN: 0-8186-3862-1. <<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3022>>

Cortadella, J.; Badia, R.M. **An asynchronous architecture model for behavioral synthesis.** *1993 European Conference on Design Automation with the European event in ASIC Design.* Institute of Electrical and Electronics Engineers (IEEE). 1993. Págs.: 307 ~ 311. ISBN/ISSN: 0-8186-3410-3.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3099>>

Badia, R.M.; Cortadella, J. **High-level synthesis of asynchronous systems: Scheduling and process synchronization.** *1993 European Conference on Design Automation with the European event in ASIC Design.* Institute of Electrical and Electronics Engineers (IEEE). 1993. Págs.: 70 ~ 74. ISBN/ISSN: 0-8186-3410-3.

<<https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=3099>>

Sánchez-Carracedo, F.; Cortadella, J. **Resource-constrained pipelining based on loop transformations.** *Euromicro 93, Open System Design: Hardware, Software and Applications: 6-9 September 1993, Barcelona: proceedings (Microprocessing and Microprogramming, vol. 38, núm. 1-5, September 1993).* Elsevier. 1993. Págs.: 429 ~ 436. ISBN/ISSN: 0165-6074. <<https://www.sciencedirect.com/journal/microprocessing-and-microprogramming/vol/38/issue/1>>

Cortadella, J.; Badia, R.M.; Pastor, E.; Pardo, A. **Achilles: a high-level synthesis system for asynchronous circuits.** *Sixth International Workshop on High Level Synthesis: Dana Point Resort, California, USA, November 4-6, 1992: workshop proceedings.* Association for Computing Machinery (ACM). 1992. Págs.: 87 ~ 94.

Cortadella, J.; Badia, R.M.; Pastor, E.; Pardo, A. **Achilles: sistema de síntesis de alto nivel para circuitos asíncronos.** *VII Congreso de Diseño de Circuitos Integrados: 3, 4 y 5 de noviembre de 1992, Toledo, España: actas.* Universidad Politécnica de Madrid (UPM). 1992. Págs.: 357 ~ 362.

Cortadella, J.; Badia, R.M. **Optimización del tiempo de ciclo en la planificación de operaciones.** *Diseño de circuitos integrados: actas del VI Congreso, Santander, 11-15 de noviembre de 1991.* Universidad de Cantabria. 1991. Págs.: 275 ~ 280. ISBN/ISSN: 84-87412-61-0.

Badia, R.M.; Cortadella, J.; Ayguade, E. **Computer-aided synthesis of data-path by using a simulated-annealing-based approach.** *Applied informatics: proceedings of the Ninth IASTED International Conference: Innsbruck, Austria, February 18-21, 1991.* ACTA Press. 1991. Págs.: 326 ~ 329. ISBN/ISSN: 0-88986-139-0.

Cortadella, J.; Jové, T. **Designing a branch target buffer for executing branches with zero time cost in a RISC processor.** *Microprocessing and Microprogramming, vol. 24, Issues 1-5, August 1988.* Elsevier. 1988. Págs.: 573 ~ 580. ISBN/ISSN: 0165-6074. <<https://www.sciencedirect.com/science/article/pii/0165607488901135>>

---

Gonzalez, A.; Llaberia, J.; Cortadella, J. **A mechanism for reducing the cost of branches in RISC architectures**. *Microprocessing & Microprogramming*, v. 24, n° 1-5. Elsevier. 1988. Págs.: 565 ~ 572. ISBN/ISSN: 0165-6074. <<http://www.sciencedirect.com/science/journal/01656074/24/1>>

Cortadella, J.; Llaberia, J. **Evaluating A+B=K conditions in constant time**. *1988 IEEE International Symposium on Circuits and Systems: Espo, Finland, 7-9 June 1988*. Institute of Electrical and Electronics Engineers (IEEE). 1988. Págs.: 243 ~ 246.

Domingo, J.; Llaberia, J.; Valero, M.; Cortadella, J. **Arbitration techniques for packet switching multistage interconnection networks**. *ICS 88: Third International Conference on Supercomputing: proceedings, Supercomputing '88*. International Supercomputing Institute. 1988. Págs.: 240 ~ 248.

Gonzalez, A.; Llaberia, J.; Cortadella, J. **Zero-delay cost branches in RISC architectures**. *Proceedings of the IASTED International Symposium Applied Informatics, AI '88*. ACTA Press. 1988. Págs.: 24 ~ 27. ISBN/ISSN: 0-88986-097-1.

Cortadella, J.; Llaberia, J. **Low cost evaluation methodology for new architectures**. *Applied Informatics '87: proceedings IASTED Symposium: Grindelwald, Switzerland, February 17-19, 1987*. ACTA Press. 1987. Págs.: 192 ~ 195. ISBN/ISSN: 0-88986-108-0.

Cortadella, J.; Llaberia, J. **An intelligent IFU for pipelined processors that makes control instructions transparent to the execution unit**. *Applied Informatics '87: proceedings IASTED Symposium: Grindelwald, Switzerland, February 17-19, 1987*. ACTA Press. 1987. Págs.: 188 ~ 191. ISBN/ISSN: 0-88986-108-0.

Domingo, J.; Llaberia, J.; Cortadella, J.; Valero, M. **Arbitration methods to increase the throughput of packet switching buffered shuffle-exchange interconnection networks**. *Applied Informatics '87: proceedings IASTED Symposium: Grindelwald, Switzerland, February 17-19, 1987*. ACTA Press. 1987. Págs.: 78 ~ 81. ISBN/ISSN: 0-88986-108-0.

González, L.; Cortadella, J.; Llaberia, J. **Performance evaluation of a loosely coupled multiprocessor architecture with two buses**. *Mini and Microcomputers and their Applications: proceedings of the ISMM International Symposium*. 1985. Págs.: 473 ~ 476.

Jové, T.; Cortadella, J. **Executing zero-delay branches with a branch target buffer in a RISC processor**. *Proceedings of the ISMM International Symposium: Mini and Microcomputers and their Applications: Sant Feliu de Guixols, Spain, June 27-30, 1988*. Servei de Publicacions de la Universitat Autònoma de Barcelona. 1985. Págs.: 373 ~ 376. ISBN/ISSN: 84-7488-121-8.

---

### A.3 Edición de libro de actas de congreso

---

### A.4 Libros

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **Logic synthesis of asynchronous controllers and interfaces**. Springer. 2002. ISBN: 978-3-642-55989-1. <<https://doi.org/10.1007/978-3-642-55989-1>>

## A.5 Capítulo de libro

---

Cortadella, J.; Sapatnekar, S. **Static timing analysis**. *Electronic design automation for integrated circuits handbook*. 2nd edition. CRC Press. 2016. ISBN: 9781482254501. <<https://www.crcpress.com/Electronic-Design-Automation-for-Integrated-Circuits-Handbook-Second-Edition/Lavagno-Markov-Martin-Scheffer/p/book/9781482254501>>

Gorgônio, K.; Cortadella, J.; Xia, F. **A compositional method for the synthesis of asynchronous communication mechanisms**. *Petri Nets and Other Models of Concurrency, ICATPN 2007, 28th International Conference on Applications and Theory of Petri Nets and Other Models of Concurrency: Siedlce, Poland, June 25-29, 2007: proceedings*. Springer. 2007. Págs.: 144 ~ 163. ISBN: 978-3-540-73093-4. <<https://doi.org/10.1007/978-3-540-73094-1>>

Kishinevsky, M.; Cortadella, J.; Grundmann, B.; Krstic, S.; O'Leary, J. **Synchronous elastic circuits**. *Computer Science, Theory and Applications: First International Computer Science Symposium in Russia, CSR 2006, St. Petersburg, Russia, June 8-12, 2006: proceedings*. Springer. 2006. Págs.: 3 ~ 5. ISBN: 978-3-540-34168-0. <<https://doi.org/10.1007/11753728>>

Carmona, J.; Cortadella, J.; Khomenko, V.; Yakovlev, A. **Synthesis of asynchronous hardware from Petri nets**. *Lectures on concurrency and Petri nets: advances in Petri nets*. Springer. 2004. Págs.: 345 ~ 401. ISBN: 978-3-540-27755-2. <<https://doi.org/10.1007/b98282>>

Carmona, J.; Cortadella, J.; Pastor, E. **Synthesis of reactive systems: application to asynchronous circuit design**. *Concurrency and hardware design: advances in Petri nets*. Springer. 2002. Págs.: 108 ~ 151. ISBN: 978-3-540-36190-9. <<https://doi.org/10.1007/3-540-36190-1>>

Kishinevsky, M.; Cortadella, J.; Kondratyev, A.; Lavagno, L.; Taubin, A.; Yakovlev, A. **Coupling asynchrony and interrupts: Place Chart Nets**. *Application and Theory of Petri Nets 1997, 18th International Conference, ICATPN'97: Toulouse, France, June 23-27, 1997: proceedings*. Springer. 1997. Págs.: 328 ~ 347. ISBN: 978-3-540-69187-7. <<https://doi.org/10.1007/3-540-63139-9>>

Sánchez-Carracedo, F.; Cortadella, J. **Resource-constrained software pipelining for high-level synthesis of DSP systems**. *Algorithms and Parallel VLSI Architectures III: proceedings of the International Workshop Algorithms and Parallel VLSI Architectures III: Leuven, Belgium, August 29-31, 1994*. Elsevier. 1995. Págs.: 377 ~ 388. ISBN: 978-0-444-82106-5. <<https://doi.org/10.1016/B978-0-444-82106-5.X5000-5>>

Roig, O.; Cortadella, J.; Pastor, E. **Verification of asynchronous circuits by BDD-based model checking of Petri nets**. *Application and Theory of Petri Nets 1995, 16th International Conference: Turin, Italy, June 26-30, 1995: proceedings*. Springer. 1995. Págs.: 374 ~ 391. ISBN: 978-3-540-49408-9. <<https://doi.org/10.1007/3-540-60029-9>>

Pastor, E.; Roig, O.; Cortadella, J.; Badia, R.M. **Petri net analysis using boolean manipulation**. *Application and Theory of Petri Nets 1994, 15th International Conference: Zaragoza, Spain, June 20-24, 1994: proceedings*. Springer. 1994. Págs.: 416 ~ 435. ISBN: 978-3-540-48462-2. <<https://doi.org/10.1007/3-540-58152-9>>

Cortadella, J.; Llaberia, J.; Valero, M. **Arquitecturas orientadas a lenguajes basados en la lógica**. *Inteligencia artificial: conceptos, técnicas y aplicaciones*. Marcombo. 1987. Págs.: 233 ~ 243. ISBN: 8426706398.

## A.6 Edición de catálogo de exposición

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## A.7 Autoría de capítulo de catálogo de exposición

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## A.8 Otros documentos científico-técnicos

---

Cortadella, J.; Lavagno, L.; Lopez, P.; Lupon, M.; Moreno, A.; Roca, A.; Sapatnekar, S. **Adaptive clock with useful jitter**. 19/05/2015. Págs.: 7. <<http://hdl.handle.net/2117/27967>>

Nikitin, N.; Cortadella, J. **Static task mapping for tiled chip multiprocessors with multiple voltage islands**. 2011. Págs.: 9. <<http://hdl.handle.net/2117/91278>>

Cortadella, J.; Gavalda, R.; Orejas, F. **Introduction to programming**. 01/09/2010. Págs.: 300. <<http://www.lsi.upc.edu/~jordicf/Teaching/programming/profes.html>>

Carmona, J.; Cortadella, J. **Process mining meets abstract interpretation**. 07/2010. Págs.: 16. <<http://hdl.handle.net/2117/88077>>

Galceran, M.; Cortadella, J.; Kishinevsky, M. **Speculation in elastic systems**. 05/2009. Págs.: 13. <<http://hdl.handle.net/2117/87919>>

Bufistov, D.; Cortadella, J.; Galceran, M.; Julvez, J.; Kishinevsky, M. **Retiming and recycling for elastic systems with early evaluation**. 04/2009. Págs.: 15. <<http://hdl.handle.net/2117/87917>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **Divide-and-conquer strategies for process mining**. 03/2009. Págs.: 20. <<http://hdl.handle.net/2117/87625>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **Region-based algorithms for process mining and synthesis of Petri nets**. 02/2009. Págs.: 14. <<http://hdl.handle.net/2117/86987>>

Carmona, J.; Cortadella, J.; Kishinevsky, M. **A recursive approach for process mining**. 02/2009. Págs.: 12.

Carmona, J.; Julvez, J.; Cortadella, J.; Kishinevsky, M. **Performance-preserving clustering of elastic controllers**. 02/2008. Págs.: 9. <<http://hdl.handle.net/2117/81941>>

Cortadella, J. **Compilers**. 01/09/2007. Págs.: 150. <<http://www.lsi.upc.edu/~jordicf/Teaching/compilers/material/>>

Cortadella, J.; Kishinevsky, M. **Synchronous elastic circuits with early evaluation and token counterflow**. 03/2007. Págs.: 13. <<http://hdl.handle.net/2117/86217>>

Cortadella, J. **Logic decomposition of incompletely specified functions**. 06/2001. Págs.: 14. <<http://hdl.handle.net/2117/97856>>

Carmona, J.; Cortadella, J. **On the realization of reactive systems**. 05/2001. Págs.: 7. <<http://hdl.handle.net/2117/97889>>

---

Carmona, J.; Cortadella, J.; Pastor, E. **A structural encoding technique for the synthesis of asynchronous circuits.** 12/2000. Págs.: 16. <<http://hdl.handle.net/2117/97626>>

Cornetta, G.; Cortadella, J. **Asynchronous NxN multipliers based on variable-delay.** 03/2000. Págs.: 20.

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Massot, M.; Moral, S.; Passerone, C.; Watanabe, Y.; Sangiovanni-Vincentelli, A. **Task generation and compile-time scheduling for mixed data-control embedded software.** 11/1999. Págs.: 44. <<http://hdl.handle.net/2117/93099>>

Cortadella, J.; Valiente, G. **A Relational view of subgraph isomorphism.** 10/1999. Págs.: 10. <<http://hdl.handle.net/2117/93081>>

Peña, M.; Cortadella, J.; Pastor, E. **Formal verification of safety properties in timed circuits.** 10/1999. Págs.: 23.

Pastor, E.; Cortadella, J. **Efficient encoding schemes for the symbolic analysis of Petri nets.** 09/1998. Págs.: 32.

Kishinevsky, M.; Cortadella, J.; Kondratyev, A.; Lavagno, L. **Asynchronous interface specification, analysis and synthesis.** 03/1998. Págs.: 17. <<http://hdl.handle.net/2117/84044>>

Sánchez-Carracedo, F.; Cortadella, J. **Reducing register pressure in software pipelining.** 11/1997. Págs.: 33.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Pastor, E.; Taubin, A.; Yakovlev, A. **Decomposition and technology mapping of speed-independent circuits using boolean relations.** 05/1997. Págs.: 19.

Cornetta, G.; Cortadella, J. **Transistor-level fault detection based on power consumption.** 05/1997. Págs.: 48.

Cornetta, G.; Cortadella, J. **Quiescent current sensing.** 05/1997. Págs.: 36.

Cornetta, G.; Cortadella, J. **Asynchronous pipelined datapaths design techniques: a survey.** 05/1997. Págs.: 31.

Cortadella, J.; Sentovich, E.; Lavagno, L. **Logic synthesis techniques for embedded control code optimization.** 03/1997. Págs.: 9.

Lavagno, L.; Cortadella, J. **Embedded code optimization via common control structure detection.** 03/1997. Págs.: 6.

Pastor, E.; Roig, O.; Cortadella, J. **Symbolic Petri net analysis using boolean manipulation.** 02/1997. Págs.: 34.

Peña, M.; Pastor, E.; Cortadella, J. **Symbolic techniques for the automatic test pattern generation for speed-independent circuits.** 01/1997. Págs.: 50.

---

Musoll, E.; Lang, T.; Cortadella, J. **Exploiting the locality of memory references to reduce the address bus energy.** 12/1996. Págs.: 9.

Semenov, A.; Yakovlev, A.; Pastor, E.; Peña, M.; Cortadella, J. **Partial order based approach to synthesis of speed-independent circuits.** 10/1996. Págs.: 25.

Semenov, A.; Yakovlev, A.; Pastor, E.; Peña, M.; Cortadella, J. **Synthesis of speed independent circuits from STG-unfolding segment.** 10/1996. Págs.: 16.

Musoll, E.; Cortadella, J. **On reducing electromagnetic interference in high-speed digital systems.** 07/1996. Págs.: 9.

Sánchez-Carracedo, F.; Cortadella, J.; Badia, R.M. **Optimal exploration of the unrolling degree for software pipelining.** 07/1996. Págs.: 16.

Pastor, E.; Cortadella, J. **Structural methods for the synthesis of speed-independent circuits.** 07/1996. Págs.: 47.

Cornetta, G.; Cortadella, J. **A survey on design quality estimation for embedded systems.** 07/1996. Págs.: 22.

Badia, R.M.; Sánchez-Carracedo, F.; Cortadella, J. **OSP: optimal software pipelining with minimum register pressure.** 06/1996. Págs.: 23.

Sánchez-Carracedo, F.; Cortadella, J. **RESIS: a new methodology for register optimization in software pipelining.** 05/1996. Págs.: 16.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Yakovlev, A.; Lavagno, L. **Coupling technology mapping, logic optimization and state encoding for speed-I.** 05/1996. Págs.: 17.

Tomas, L.; Lang, T.; Musoll, E.; Cortadella, J. **Individual flip-flops with gated clocks for low-power datapaths.** 01/1996. Págs.: 23.

Tomas, L.; Lang, T.; Musoll, E.; Cortadella, J. **Redundant adder for reduced output transitions.** 01/1996. Págs.: 13.

Cortadella, J.; Kishinevsky, M.; Lavagno, L.; Yakovlev, A. **Deriving Petri nets from finite transition systems.** 01/1996. Págs.: 34.

Tomas, L.; Lang, T.; Musoll, E.; Cortadella, J. **Reducing energy consumption of flip-flops.** 01/1996. Págs.: 20.

Peña, M.; Cortadella, J. **Combining process algebras and Petri nets for the specification and synthesis of asynchronous circuits.** 12/1995. Págs.: 30.

Cortadella, J.; Kishinevsky, M.; Kondratyev, A.; Lavagno, L.; Yakovlev, A. **A region-based theory for state assignment in asynchronous circuits.** 10/1995. Págs.: 80.

---

Cortadella, J.; Badia, R.M.; Sánchez-Carracedo, F. **A mathematical formulation of the loop pipelining problem.** 10/1995. Págs.: 25.

Pastor, E.; Cortadella, J.; Kondratyev, A.; Roig, O. **Structural algorithms for the synthesis of speed-independent circuits from signal transition graphs.** 10/1995. Págs.: 54.

Cortadella, J.; Badia, R.M.; Sánchez-Carracedo, F. **A mathematical formulation of the loop pipelining problem.** 06/1995. Págs.: 25.

Pastor, E.; Cortadella, J.; Kondratyev, A.; Roig, O. **Structural algorithms for the synthesis of speed-independent circuits from signal transition graphs.** 05/1995. Págs.: 55.

Sánchez-Carracedo, F.; Cortadella, J. **Time-constrained loop pipelining.** 02/1995. Págs.: 99.

Sánchez-Carracedo, F.; Cortadella, J. **Register optimization for maximum throughput loop pipelining.** 01/1995. Págs.: 99.

Cortadella, J.; KISHINEVKY, M.; Lavagno, L.; Yakovlev, A. **Synthesizing Petri nets from state-based models.** 01/1995. Págs.: 36.

Cortadella, J. **Mapping BDD'S into DCVSL gates.** 01/1995. Págs.: 10.

Roig, O.; Cortadella, J.; Pastor, E. **Hierarchical gate-level verification of speed-independent circuits.** 01/1995. Págs.: 15.

Roig, O.; Cortadella, J.; Pastor, E. **Symbolic model checking of Petri nets for the verification of speed-independent circuits.** 12/1994. Págs.: 60.

Sánchez-Carracedo, F.; Cortadella, J. **Maximum throughput loop pipelining with register optimization.** 10/1994. Págs.: 20.

Pastor, E.; Cortadella, J.; Roig, O. **A new look at the conditions for the synthesis of speed-independent circuits.** 10/1994. Págs.: 60.

Sánchez-Carracedo, F.; Cortadella, J. **Unrolling and retiming: a new approach for resource-constrained software pipelining.** 08/1994. Págs.: 74.

Sánchez-Carracedo, F.; Cortadella, J. **UNRET: A transformation-based technique for software pipelining with resource constraints.** 07/1994. Págs.: 16.

Roig, O.; Cortadella, J.; Pastor, E. **Conservative symbolic model-checking of Petri nets for speed-independent circuits.** 07/1994. Págs.: 15.

Cortadella, J.; Gonzalez, A.; Jerez, T.; Llosa, J.; Parcerisa, Joan-Manuel; Valero, M. **Comparative study of numerical applications on the ACRI-1 architecture. Deliverable: June 1993 - May 1994.** 05/1994. Págs.: 38.

---

Cortadella, J.; Lavagno, L.; Vanbekbergen, P.; Yakovlev, A. **Designing asynchronous circuits from behavioural specifications with internal conflicts**. 05/1994. Págs.: 20.

Cortadella, J. **Disseny bàsic VLSI**. 09/1993. Págs.: 95.

Cortadella, J.; Gonzalez, A.; Parcerisa, Josep; Valero-Garcia, M **Linear algebra routines and FFT on the ACRI architectures**. 06/1993. Págs.: 68.

Sánchez-Carracedo, F.; Cortadella, J. **RLCP: a novel approach for resource-constrained loop pipelining**. 05/1993. Págs.: 46.

Pastor, E.; Cortadella, J. **P-time unique state coding algorithms for signal transition graphs**. 05/1993. Págs.: 0.

Pastor, E.; Roig, O.; Cortadella, J. **TRISC: diseño de un procesador RISC de 32 bits**. 10/1992. Págs.: 0.

Badia, R.M.; Cortadella, J. **High-level synthesis of asynchronous digital circuits scheduling**. 09/1992. Págs.: 0.

Cortadella, J.; Del Corral, A.; Elias, E. **Specification of the police criterion chip (final)**. 03/1992. Págs.: 30.

Del Corral, A.; Cortadella, J.; Elias, E. **Manual de usuario del chip de policía**. 11/1991. Págs.: 18.

Cortadella, J.; Badia, R.M. **High-level synthesis of asynchronous systems**. 10/1991. Págs.: 0.

Cortadella, J.; Del Corral, A.; Elias, E. **Specification of the police criterion chip (frozen)**. 06/1991. Págs.: 31.

Elias, A.; Del Corral, A.; Cortadella, J. **Police criterion chip: testing**. 06/1991. Págs.: 6.

Del Corral, A.; Elias, E.; Cortadella, J. **Descripción estructural del chip de policía**. 05/1991. Págs.: 28.

Cortadella, J. **Police criterion chip: final design report**. 02/1991. Págs.: 7.

Cortadella, J. **Specification of the police criterion chip**. 05/1990. Págs.: 23.

Cortadella, J.; Martin, J. **Surveillance circuit for the police criterion chip**. 05/1990. Págs.: 7.

Cortadella, J. **Specification of the police criterion chip**. 01/1990. Págs.: 20.

Cortadella, J. **Specification of the police criterion chip (version 2.0)**. 01/1990. Págs.: 15.

Cortadella, J. **Specification of the police criterion chip (revised version)**. 10/1989. Págs.: 10.

---

Cortadella, J. **Specification of the police criterion chip**. 09/1989. Págs.: 0.

Gonzalez, A.; Llaberia, J.; Cortadella, J. **A mechanism for reducing the cost of branches in RISC architectures**. 12/1987. Págs.: 60.

Cortadella, J.; Llaberia, J.; Gonzalez, A. **Keeping control transfer instructions out of the pipeline in architectures without condition codes**. 05/1987. Págs.: 60. <<http://hdl.handle.net/2117/110641>>

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## **A.9 Trabajos académicos**

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### **A.10 Manual-apuntes**

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Burgues, X.; Cortadella, J.; Esteban, J. L.; Galesi, N.; Martinez, E.; Orejas, F.; Rubio, A. **Programació 1 (notes de curs)**. Apuntes. 2001.

Cortadella, J.; Badia, R.M.; Pastor, E. **Transparències de l'assignatura (DBVLSI)**. Apuntes. 1998.

Cortadella, J.; Badia, R.M. **Apunts (SAC)**. Apuntes. 1996.

Cortadella, J.; Badia, R.M. **Apunts (DBVLSI)**. Apuntes. 1996.

Cortadella, J. **Apunts (DBVLSI)**. Apuntes. 1995.

Cortadella, J.; Badia, R.M. **Documentació de pràctiques i de problemes (DBVLSI)**. Prácticas de laboratorio. 1995.

Cortadella, J.; Ayguade, E. **Apunts (DBVLSI)**. Apuntes. 1995.

Cortadella, J. **Apunts (DBVLSI)**. Apuntes. 1995.

Cortadella, J.; Badia, R.M. **Documentació de pràctiques i problemes (DBVLSI)**. Prácticas de laboratorio. 1995.

Cortadella, J.; Badia, R.M. **Documentació de pràctiques i de problemes (assignatura DBVLSI)**. Prácticas de laboratorio. 1994.

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## **A.11 Otra producción documental / Preprints**

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## B. Congresos, cursos y otros eventos

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### B.1 Presentaciones de trabajos en congresos

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Cortadella, J. **Hazard-free logic synthesis and technology mapping.** *Summer School on Asynchronous Circuit Design 2002.* 15/07/2002.

Cortadella, J. **Synthesis of embedded software for reactive systems.** *1st Integration of Software Specification Techniques Workshop.* 06/04/2002.

Cortadella, J. **A relational view of subgraph isomorphism.** *5th International Seminar on Relational Methods in Computer Science.* 09/01/2000.

Cortadella, J. **Behavioral transformations to increase the noise immunity of asynchronous specifications.** *Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems.* 19/04/1999.

Cortadella, J. **Crosstalk noise avoidance in asynchronous circuits.** *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems.* 08/03/1999.

Cortadella, J. **Lazy transition systems: application to timing optimization of asynchronous circuits.** *1998 IEEE/ACM International Conference on Computer Aided Design.* 09/11/1998.

Cortadella, J. **Extension of the working-zone-encoding method to reduce the energy on the microprocessor data bus.** *1998 IEEE International Conference on Computer Design: VLSI in Computers and Processors.* 05/10/1998.

Cortadella, J. **Reducing the energy of address and data buses with the working-zone encoding technique and its effect on multimedia applications.** *1998 Power Driven Microarchitecture Workshop.* 28/06/1998.

Cortadella, J. **Automatic handshake expansion and reshuffling using concurrency reduction.** *1st Workshop on Hardware Design and Petri Nets.* 23/06/1998.

Cortadella, J. **Asynchronous circuit verification and synthesis with Petri nets.** *1st Workshop on Hardware Design and Petri Nets.* 23/06/1998.

Cortadella, J. **Asynchronous interface specification, analysis and synthesis.** *35th Design Automation Conference.* 16/06/1998.

Cortadella, J. **Identifying state coding conflicts in asynchronous system specifications using Petri net unfoldings.** *1st International Conference on Application of Concurrency to System Design.* 26/03/1998.

Cortadella, J. **Combining structural and symbolic methods for the verification of concurrent systems.** *1st International Conference on Application of Concurrency to System Design.* 24/03/1998.

---

Cortadella, J. **Efficient encoding schemes for symbolic analysis of Petri nets.** *Design, Automation and Test in Europe 1998.* 25/02/1998.

Cortadella, J. **Chairman de sessió.** *1997 IEEE/ACM International Conference on Computer Aided Design.* 09/11/1997.

Cortadella, J. **Decomposition and technology mapping of speed-independent circuits.** *1997 IEEE/ACM International Conference on Computer Aided Design.* 09/11/1997.

Cortadella, J. **Coupling asynchrony and interrupts: Place Chart Nets and their synthesis.** *International Conference on Application and Theory of Petri Nets.* 23/06/1997.

Cortadella, J. **Automatic generation of synchronous test patterns for asynchronous circuits.** *Design Automation Conference.* 09/06/1997.

Cortadella, J. **Synthesis of speed-independent circuits from STG-unfolding segment.** *Design Automation Conference.* 09/06/1997.

Cortadella, J. **Redundant adder for reduced output transitions.** *XI Design of Integrated Circuits and Systems Conference.* 20/11/1996.

Cortadella, J. **Petrify a tool for manipulating concurrent specifications and sybthesis of asynchronous controllers..** *XI Design of Integrated Circuits and Systems Conference.* 20/11/1996.

Cortadella, J. **A mathematical formulation of the loop pipelining problem.** *XI Design of Integrated Circuits and Systems Conference.* 20/11/1996.

Cortadella, J. **Flujo de diseño asíncrono con la biblioteca DCVSL\_LIB para ES2 ECPD10.** *II Congreso sobre Tecnologías Aplicadas a la Enseñanza de la Electrónica.* 19/09/1996.

Cortadella, J. **RESIS: A new methodology for register optimization in software pipelining.** *2nd International European Conference on Parallel Processing.* 26/08/1996.

Cortadella, J. **Methodology and tools for state encoding in asynchronous circuit synthesis.** *33rd Design Automation Conference.* 03/06/1996.

Cortadella, J. **Maximum-throughput software pipelining.** *2nd International Conference on Massively Parallel Computing Systems.* 06/05/1996.

Cortadella, J. **Complete state encoding based on the theory of regions.** *2nd International Symposium on Advanced Research in Asynchronous Circuits and Systems.* 18/03/1996.

Cortadella, J. **Combining process algebras and Petri nets for the specification and synthesis of asynchronous circuits.** *2nd International Symposium on Advanced Research in Asynchronous Circuits and Systems.* 18/03/1996.

---

Cortadella, J. **Optimizing CMOS circuits for low power using transistor reordering.** *European Design and Test Conference 1996.* 11/03/1996.

Cortadella, J. **Structural methods for the synthesis of speed-independent circuits.** *European Design and Test Conference 1996.* 11/03/1996.

Cortadella, J. **Cover approximations for the synthesis of speed-independent circuits.** *International Workshop on Logic and Architecture Synthesis 1995.* 18/12/1995.

Cortadella, J. **Programación VLSI y síntesis de circuitos asíncronos mediante composición de redes de Petri.** *X Congreso de Diseño de Circuitos Integrados y Sistemas.* 15/11/1995.

Cortadella, J. **Synthesizing Petri nets from state-based models.** *1995 IEEE/ACM International Conference on Computer Aided Design.* 05/11/1995.

Cortadella, J. **Time-constrained loop pipelining.** *1995 IEEE/ACM International Conference on Computer-Aided Design.* 05/11/1995.

Cortadella, J. **Low-power array multipliers with transition-retaining barriers.** *International Workshop on Power and Timing Modeling Optimization and Simulation 1995.* 20/10/1995.

Cortadella, J. **Scheduling and resource binding for low power.** *Eight International Symposium on System Synthesis.* 13/09/1995.

Cortadella, J. **Verification of asynchronous circuits by BDD-based model checking of Petri nets.** *16th International Conference on Application and Theory of Petri Nets.* 26/06/1995.

Cortadella, J. **Hierarchical gate-level verification of speed-independent circuits.** *Second Working Conference on Asynchronous Design Methodologies.* 30/05/1995.

Cortadella, J. **High-level synthesis techniques for reducing the activity of functional units.** *1995 International Symposium on Low Power Design.* 23/04/1995.

Cortadella, J. **A new look at the conditions for the synthesis of speed-independent circuits.** *Fifth Great Lakes Symposium on VLSI.* 16/03/1995.

Cortadella, J. **Checking signal transition graph implementability by symbolic BDD traversal.** *The European Design and Test Conference ED&TC 1995.* 06/03/1995.

Cortadella, J. **Designing asynchronous circuits from behavioural specifications with internal.** *International Symposium on Advanced Research in Asynchronous Circuits and Systems 1994.* 03/11/1994.

Cortadella, J. **A systematic approach to design asynchronous circuits with internal conflicts.** *ACiD-WG Workshop on Testing and Design for Testability.* 26/09/1994.

---

Cortadella, J. **Resource-constrained software pipelining for high-level synthesis of DSP systems**. *3rd International Workshop on Algorithms and Parallel VLSI Architectures*. 29/08/1994.

Cortadella, J. **Symbolic model checking of petri nets for speed-independent circuits**. *ACiD-WG Workshop in Asynchronous Low-Power VLSI*. 11/04/1994.

Cortadella, J. **Síntesis de máquinas de control para circuitos asíncronos**. *DCIS 1993 (VIII Congreso de Diseño de Circuitos Integrados)*. 09/11/1993.

Cortadella, J. **Polynomial algorithms for the synthesis of hazard-free circuits from STGs**. *1993 IEEE/ACM International Conference on Computer Aided Design*. 07/11/1993.

Cortadella, J. **Control distribution from high-level descriptions**. *ACiD-WG EXACT Workshop on Asynchronous Controllers and Interfacing 1992*. 02/09/1992.

Cortadella, J. **Designing the TRISC microprocessor: from ELLA to layout**. *10th ELLA User Group*. 01/05/1990.

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## B.2 Impartición de cursos y seminarios

**Criteris per avaluar els aspectes ètics i de protecció de dades vinculats a la recerca educativa**. *Criteris per avaluar els aspectes ètics i de protecció de dades vinculats a la recerca educativa*. Instituto de Ciencias de la Educación. Barcelona, España. 2025.

**Synthesis of control circuits from STG specifications**. *Synthesis of control circuits from STG specifications*. , Dinamarca. 1997.

**A region-based theory for state assignment of asynchronous circuits**. *A region-based theory for state assignment of asynchronous circuits*. Estados Unidos de América. 1995.

**Synthesis techniques for low-power circuits**. *Synthesis techniques for low-power circuits*. Japón. 1995.

**Division: Multiplicative and Digit-recurrent algorithms**. *Division: Multiplicative and Digit-recurrent algorithms*. Japón. 1995.

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## B.3 Impartición de conferencias

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## B.4 Colaboración en exposiciones

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## B.5 Organización de ediciones de congreso

**Altres: Reversible and Asynchronous Computation - Jia Lee**. Barcelona, España. 2004.

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**Altres: Nanocomputing by Asynchronous Systems - Ferdinand Peper.** Barcelona, España. 2004.

**Organitzador Principal: FIFTH INTERNATIONAL SYMPOSIUM ON ADVANCED RESEARCH IN ASYNCHRONOUS CIRCUITS AND SYSTEMS - ASYNC'99.** Barcelona. 1998.

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## **B.6 Organización de cursos o seminarios**

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**Organitzador Principal: Javier Campos: Course: Modelado y análisis de sistemas concurrentes con redes de Petri. Evaluación de rendimiento.** 2007. Barcelona.

**Organitzador Principal: Sachin Sapatnekar: Solving [Specific Classes of] Linear Equations using Random Walks.** 2007. Barcelona.

**Organitzador Principal: Sachin Sapatnekar: Automated Physical Design for VLSI Circuits (V).** 2006. Barcelona.

**Altres: Automated Physical Design for VLSI Circuits (V).** 2006. Barcelona.

**Organitzador Principal: Sachin Sapatnekar: Automated Physical Design for VLSI Circuits (IV).** 2006. Barcelona.

**Altres: Automated Physical Design for VLSI Circuits (IV).** 2006. Barcelona.

**Organitzador Principal: Sachin Sapatnekar: Automated Physical Design for VLSI Circuits (III).** 2006. Barcelona.

**Altres: Automated Physical Design for VLSI Circuits (III).** 2006. Barcelona.

**Altres: Automated Physical Design for VLSI Circuits (II).** 2006. Barcelona.

**Organitzador Principal: Automated Physical Design for VLSI Circuits.** 2006.

**Altres: Automated Physical Design for VLSI Circuits (I).** 2006. Barcelona.

**Altres: Advanced Topics on Algorithmics and Complexity.** 2006. Barcelona.

**Altres: Synchronous elastic networks.** 2006. Barcelona.

**Altres: Nanocomputing: a new paradigm for long-term research.** 2006. Barcelona.

**Organitzador Principal: Algebraic Techniques for the Analysis and control of continuous Petri Nets.** 2005. Barcelona.

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**Organitzador Principal: High-level design and verification using the synchronous language Esterel.** 2005. Barcelona.

**Organitzador Principal: Research at strategic CAD Labs (Intel Corporation).** 2005. Barcelona.

**Altres: Reversible and Asynchronous Computation.** 2004. Barcelona.

**Altres: Nanocomputing by Asynchronous Systems.** 2004. Barcelona.

**Organitzador Principal: Reversible and Asynchronous Computation - Jia Lee.** 2004. Barcelona.

**Organitzador Principal: Nanocomputing by Asynchronous Systems - Ferdinand Peper.** 2004. Barcelona.

**Organitzador Principal: Scenario-Based Methods for System Design - P.S. Thiagarajan.** 2003. Barcelona.

**Organitzador Principal: Reuse of Coloured Petri Net Models - Angelo Perkusich.** 2003. Barcelona.

**Organitzador Principal: Symbolic Reachability Analysis using Implicit Additive Decomposition - Supratik Chakraborty.** 2003. Barcelona.

**Organitzador Principal: Abstracci3n Autom3tica de Sistemas Secuenciales - Abelardo Pardo.** 2001. Barcelona.

**Organitzaci3/Direcci3: Synthesis of control circuits from STG specifications.** 1997. , Dinamarca.

**Organitzador Principal: DESIGNING A SELF-TIMED TOKEN RING FOR DISTRIBUTED SYSTEMS.** 1995.

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## **B.7 Organizaci3n de ediciones de premios**

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## **B.8 Pertenencia a comit3 cient3fico de un congreso**

**Presidente. Comit3 de la edici3 del congres Workshop on Token Based Computing:** *Workshop on Token Based Computing.* Bologna, Italia. 22/06/2004 - 22/06/2004.

**Vocal. Comit3 de la edici3 del congres Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems:** *Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems.* Eilat, Israel. 02/04/2000 - 02/04/2000.

**Otros. Comit3 de la edici3 del congres IEEE/ACM International Conference on Computer Aided Design:** *IEEE/ACM International Conference on Computer Aided Design 1999.* San Jose, CA, Estados Unidos de Am3rica. 07/11/1999 - 07/11/1999.

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**Vocal. Comitè de la edició del congres IEEE/ACM International Conference on Computer Aided Design:** *1997 IEEE/ACM International Conference on Computer Aided Design*. San Jose, CA, Estados Unidos de América. 09/11/1997 - 09/11/1997.

**Otros. Comitè Científic de la edició del congres 33rd Design Automation Conference 1996:** *33rd Design Automation Conference*. Las Vegas, NV, Estados Unidos de América. 03/06/1996 - 03/06/1996.

**Vocal. Comitè de la edició del congres Second Working Conference on Asynchronous Design Methodologies:** *Second Working Conference on Asynchronous Design Methodologies*. London, Reino Unido. 30/05/1995 - 30/05/1995.

**Vocal. Comitè Científic de la edició del congres Modeling and Simulation ESM 94:** *Modeling and Simulation ESM 94*. España. 01/06/1994 - 01/06/1994.

**Otros. Comitè Científic de la edició del congres II International Workshop on Massive Parallelism: Hardware, Software and Appli:** *II International Workshop on Massive Parallelism: Hardware, Software and Appli*. Italia. 01/06/1994 - 01/06/1994.

**Otros. Comitè Científic de la edició del congres DCIS 1994 (IX Congreso de Diseno de Circuitos Integrados:** *DCIS 1994 (IX Congreso de Diseno de Circuitos Integrados*. España. 20/05/1994 - 20/05/1994.

**Otros. Comitè Científic de la edició del congres EUROMICRO 94:** *EUROMICRO 94*. Reino Unido. 01/03/1994 - 01/03/1994.

**Otros. Comitè de la edició del congres 27th Annual Hawaii International Conference on System Sciences:** *27th Annual Hawaii International Conference on System Sciences*. Estados Unidos de América. 04/01/1994 - 04/01/1994.

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## B.9 Asistencia a curso o seminario

**Com introduir l'ètica a la teva docència?** Barcelona, España. 2024.

**I Jornada Docent del Departament de Ciències de la Computació.** Barcelona, España. 2024.

**Reunió de coordinació docent del Grau en Matemàtiques.** Barcelona, España. 2017.

**A region-based theory for state assignment of asynchronous circuits.** Estados Unidos de América. 1995.

**Synthesis techniques for low-power circuits.** Japón. 1995.

**Division: Multiplicative and Digit-recurrent algorithms.** Japón. 1995.

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## C. Proyectos y propiedad intelectual o industrial

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## C.1 Participación en proyecto IDi competitivo

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**Investigador. Chips para arquitecturas avanzadas y sistemas fotónicos.** Coordinador científico: Rubio, A.. 12/09/2023 - 30/06/2026. Duración: 02 año/s 09 mes/es 19 día/s . Financiación: 3.761.798,45 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ingeniería Electrónica. Entidad financiadora: MIN DE ECONOMIA Y COMPETITIVIDAD.

**Investigador. Algorismia, Bioinformatica, Complejidad y Métodos Formales.** Coordinador científico: Serna, M.. 01/01/2022 - 30/06/2025. Duración: 03 año/s 06 mes/es . Financiación: 0,00 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

**Investigador. Modelos y Técnicas para el Procesamiento de Información a Gran Escala -- Barcelona.** Coordinador científico: Carmona, J.; Orejas, F.; Serna, M.. 01/09/2021 - 31/08/2026. Duración: 05 año/s . Financiación: 363.000,00 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGENCIA ESTATAL DE INVESTIGACION.

**Investigador. Modelos y métodos basados en grafos para la computación en gran escala.** Coordinador científico: Carmona, J.; Orejas, F.. 01/01/2018 - 30/09/2021. Duración: 03 año/s 09 mes/es . Financiación: 250.373,42 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGENCIA ESTATAL DE INVESTIGACION.

**Investigador. Algorismia, Bioinformàtica, Complexitat i Mètodes Formals.** Coordinador científico: Orejas, F.; Diaz, J.. 01/01/2017 - 30/09/2021. Duración: 04 año/s 09 mes/es . Financiación: 23.989,15 €. Ámbito: Autonómico. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

**Investigador. Algorismia, Bioinformàtica, Complexitat i Mètodes Formals ALBCOM.** Coordinador científico: Diaz, J.. 01/01/2014 - 30/04/2017. Duración: 03 año/s 04 mes/es . Financiación: 45.000,00 €. Ámbito: Autonómico. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

**Investigador. Modelos y métodos computacionales para datos masivos estructurados.** Coordinador científico: Orejas, F.. 01/01/2014 - 31/12/2017. Duración: 04 año/s . Financiación: 292.697,08 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: MIN DE ECONOMIA Y COMPETITIVIDAD.

**Investigador. ALGORISMIA, BIOINFORMÀTICA, COMPLEXITAT I METODES FORMALS (ALBCOM).** Coordinador científico: Diaz, J.. 25/09/2009 - 30/04/2014. Duración: 04 año/s 07 mes/es 06 día/s . Financiación: 58.240,00 €. Ámbito: Autonómico. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

**Investigador. Métodos formales y algoritmos para el diseño de sistemas.** Coordinador científico: Orejas, F.. 01/10/2007 - 30/09/2012. Duración: 04 año/s 11 mes/es 29 día/s . Financiación: 1.072.060,00 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: CICYT TIN2007-66523.

**Coordinador científico. ACID WG Working group on asynchronous circuit design.** Coordinador científico: Cortadella, J.; Junyent, G.. 27/10/2000 - 31/08/2004. Duración: 03 año/s 10 mes/es 09 día/s . Financiación: 20.016,00 €. Ámbito: Europeo. Entidad donde se desarrolla: Departamento de Ciencias de la Computación.

**Coordinador científico. Subvencio per a la recerca en l'area de metodologia i eines per a l'especificacio, sintesi i verificacio de circuits asincronics amb temps relatiu.** Coordinador científico: Cortadella, J..

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18/08/1999 - 31/08/2000. Duración: 01 año/s 14 día/s . Financiación: 38.464,77 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: INTEL CORPORATION.

**Coordinador científico. Fith International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC99).** Coordinador científico: Cortadella, J.. 30/12/1998 - 30/12/1999. Duración: 01 año/s . Financiación: 6.010,12 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: DGES (ANTIGA DGICYT).

**Coordinador científico. Metodos formales para la sintesis y verificacion de sistemas concurrentes.** Coordinador científico: Cortadella, J.. 30/11/1998 - 29/11/2001. Duración: 03 año/s . Financiación: 67.241,24 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: CICYT.

**Coordinador científico. Cosy - codesign simulation and synthesis.** Coordinador científico: Cortadella, J.. 01/10/1997 - 31/03/2000. Duración: 02 año/s 06 mes/es 02 día/s . Financiación: 109.083,70 €. Ámbito: Europeo. Entidad donde se desarrolla: Departamento de Ciencias de la Computación.

**Coordinador científico. ACiD-WG. Asynchonus circuit design.** Coordinador científico: Cortadella, J.. 06/06/1996 - 13/09/1998. Duración: 02 año/s 03 mes/es 09 día/s . Financiación: 15.866,72 €. Ámbito: Europeo. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores.

**Coordinador científico. Herramientas de CAD para síntesis de circuitos digitales asíncronos.** Coordinador científico: Cortadella, J.. 10/04/1996 - 15/12/1997. Duración: 01 año/s 08 mes/es 09 día/s . Financiación: 0,00 €. Ámbito: Estatal. Entidad donde se desarrolla: Si us plau, indiqueu l'entitat on es desenvolupa. Entidad financiadora: UK HB1995-0203, ACCIONES INTEGRADAS ESPAÑA-REINO UNIDO, MINISTERIO DE .

**Coordinador científico. Arquitecturas de alta velocidad y bajo consumo para aplicaciones de proposito especifico.** Coordinador científico: Cortadella, J.. 01/07/1995 - 01/07/1998. Duración: 03 año/s 01 día/s . Financiación: 78.672,49 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

**Coordinador científico. Diseño y verificacion de circuitos de bajo consumo y alto rendimiento..** Coordinador científico: Cortadella, J.. 14/06/1994 - 14/06/1995. Duración: 01 año/s . Financiación: 15.025,30 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

**Coordinador científico. Fifth international conference on advanced research in asynchronous circuits and systems.** Coordinador científico: Cortadella, J.. 13/05/1993 - 13/05/1996. Duración: 03 año/s 01 día/s . Financiación: 2.404,04 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: CICYT.

**Coordinador científico. Congreso internacional euromicro-93.** Coordinador científico: Cortadella, J.. 01/04/1993 - 01/04/1994. Duración: 01 año/s . Financiación: 6.010,12 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

**Coordinador científico. Acid WG-asynchronous circuit design.** Coordinador científico: Cortadella, J.. 02/06/1992 - 30/12/1995. Duración: 03 año/s 07 mes/es 01 día/s . Financiación: 0,00 €. Ámbito: Estatal. Entidad donde se desarrolla: Si us plau, indiqueu l'entitat on es desenvolupa. Entidad financiadora: ESPRIT 7225.

**Coordinador científico. Arquitecturas paralelas orientadas a aplicaciones simbolicas.** Coordinador científico: Cortadella, J.. 01/01/1991 - 31/12/1993. Duración: 03 año/s . Financiación: 109.720,77 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

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**Coordinador científico. Diseño y evaluación de arquitecturas orientadas a lenguajes de alto nivel.**

Coordinador científico: Cortadella, J.. 31/12/1989 - 31/12/1991. Duración: 02 año/s . Financiación: 106.739,75 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

**Coordinador científico. Disseny i avaluació d'arquitectures orientades a ....**

Coordinador científico: Cortadella, J.. 01/01/1989 - 31/12/1990. Duración: 01 año/s 12 mes/es 04 día/s . Financiación: 106.739,75 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores. Entidad financiadora: CICYT.

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**C.2 Participación en proyecto IDi no competitivo**

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**Coordinador científico. Algorithm for CAD Flow research.** Coordinador científico: Cortadella, J.. 28/09/2022 - 31/12/2023. Duración: 01 año/s 03 mes/es 04 día/s . Financiación: 22.756,25 €. Ámbito: Internacional. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: QUALCOMM INC.

**Coordinador científico. Macro floorplanning and dataflow automatic analysis for ASICs.** Coordinador científico: Cortadella, J.. 05/02/2018 - 05/08/2018. Duración: 06 mes/es 01 día/s . Financiación: 25.000,00 €. Ámbito: Internacional. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: ESILICON ROMANIA SRL.

**Coordinador científico. Support the research in the area of/'Macro floorplanning and dataflow automatic analysis for ASICs/'.** Coordinador científico: Cortadella, J.. 17/02/2017 - 02/02/2018. Duración: 11 mes/es 17 día/s . Financiación: 18.000,00 €. Ámbito: Autonómico. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: ESILICON ROMANIA SRL.

**Investigador. Realización de un ensayo cuyo objetivo es estudiar la viabilidad del proceso de automatización de detección de fraudes o irregularidades en los sistemas de información de Gas Natural..**

Coordinador científico: Carmona, J.. 30/09/2013 - 31/12/2019. Duración: 06 año/s 03 mes/es 02 día/s . Financiación: 646.502,47 €. Ámbito: Estatal. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: LEAN GRIDS SERVICES SL.

**Coordinador científico. Suport a la recerca Intel.** Coordinador científico: Cortadella, J.. 20/03/2012 - 31/12/2014. Duración: 02 año/s 09 mes/es 12 día/s . Financiación: 54.457,07 €. Ámbito: Internacional. Entidad donde se desarrolla: Departamento de Ciencias de la Computación. Entidad financiadora: INTEL CORPORATION.

**Coordinador científico. DESIGN AUTOMATION FOR EMBEDDED ELECTRONIC SYSTEM.** Coordinador científico: Cortadella, J.. 05/12/2000 - 30/11/2003. Duración: 02 año/s 12 mes/es . Financiación: 45.676,92 €. Entidad donde se desarrolla: Departamento de Ciencias de la Computación.

**Investigador. "Technology for ATD", Proyecto RACE 1022.** Coordinador científico: Domingo, J.. 20/12/1988 - 20/12/1992. Duración: 04 año/s 01 día/s . Financiación: 416.509,72 €. Entidad donde se desarrolla: Departamento de Arquitectura de Computadores.

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**C.3 Participación en proyectos de innovación docente**

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**Colaborador/a: Eines per a la Transformació de la Docència en Programació.** Investigador responsable: Valiente, G. 01/09/2024 - 31/12/2025. Duración: 01 año/s 04 mes/es . Proyecto de innovación o mejora docente financiado. Entidad financiadora: Universitat Politècnica de Catalunya.

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#### C.4 Titularidad de propiedad industrial o intelectual

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Cortadella, J. **A method for increasing the operating frequency of synchronous digital circuits using a single clock tree and a mixed distribution of sequential elements..** Número de registro: **IT102023000006735. Patente invención.** Fecha de registro: 05/04/2023. País de registro: Italia. Ámbito: Europeo. Entidad titular: Politecnico di Torino.

Cortadella, J. **Adaptive Clocking Configurations and Calibration Methods Thereof.** Número de registro: **PCT/EP2014/058457. Patente invención.** Fecha de registro: 25/04/2014. País de registro: España. Ámbito: Internacional. Entidad titular: Universitat Politècnica de Catalunya.

Cortadella, J.; Lavagno, L.; Tuncer, E. **Network of tightly coupled performance monitors for determining the maximum frequency of operation of a semiconductor IC.** Breve descripción: A circuit interconnection structure for synchronizing a network of oscillators placed on a semiconductor substrate. One such structure comprises a first synchronizing circuit electrically coupled to a second synchronizing circuit through tunable delay circuits. Also disclosed are methods to tune oscillators placed in different regions of a circuit having multiple clock domains by estimating the relative slack of a first group of signals within the circuit with regard to the period of a first clock domain, and estimating the relative slack of the second group of signals within the circuit with regard to the period of second clock domain, wherein the estimating is performed at process and operational corners that cover the variability of the circuit at different speed conditions, then calculating tuning values for the oscillator delays for each region such that the oscillator delay slack matches the worst relative slack of the signals of the same region.. Número de registro: **US 13/181,362. Patente invención.** Fecha de registro: 12/07/2010. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: eSilicon Corporation.

Cortadella, J.; Lavagno, L.; Macián, C.; Martorell, F. **Asynchronous scheme for clock domain crossing.** Breve descripción: Apparatus and methods for clock domain crossing between a first clock domain and a second clock domain. The apparatus comprises a first control logic element for processing a handshake signal and producing a first arbiter input signal. Concurrently a second control logic element processes a second handshake signal and produces a second arbiter input signal. Exemplary embodiments include exactly one arbiter element inputting the first arbiter input signal, inputting the second arbiter input signal, outputting a first clocking signal to the first sequential element and outputting a second clocking signal to the second sequential element. For managing metastability by controlling the timing of the clocking inputs of the sequential devices, the apparatus includes a first controllable lock delay element selected to satisfy the setup constraint of the second sequential element, and a second controllable lock delay element selected to satisfy the hold constraint of the second sequential element.. Número de registro: **US 12/711,909. Patente invención.** Fecha de registro: 24/02/2010. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: eSilicon Corporation.

Cortadella, J.; Singhal, V.; Tuncer, E. **Variability-aware scheme for asynchronous circuit initialization.** Breve descripción: A system for automatically transforming a given synchronous circuit description into an equivalent and provably correct desynchronized circuit description. Included in the automated transformation are techniques for synthesizing a variability-aware controller using a two-phase protocol, techniques for synthesizing a variability-aware controller using gated clocks and testability circuits, techniques for synthesizing a variability-aware controller optimized for performance, techniques for initializing the synthesized controller, techniques for dynamically minimizing power requirements, and techniques for interfacing the desynchronized circuit with external synchronous circuits. Also disclosed are techniques for implementing a system for automatically transforming a synchronous circuit description into an equivalent and provably correct desynchronized circuit description within the context of an electronic design automation design flow.... Número de registro: **US 12/265,571. Patente invención.** Fecha de registro: 06/11/2007. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: Elastix Corporation.

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Cortadella, J.; Kishinevsky, M. **Synchronous elastic designs with early evaluation**. Breve descripción: Embodiments of early enabling synchronous elastic designs, devices and methods are presented herein.. Número de registro: **US 11/634,462. Patente invención**. Fecha de registro: 06/12/2006. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: Intel Corporation.

Cortadella, J.; Kondratyev, A.; Lavagno, L. **Skew insensitive clocking method and apparatus**. Breve descripción: A method of designing a skew insensitive circuit is performed by designing a synchronous circuit including flip-flops and combinatorial logic and, for each flip-flop, inserting logic gates to receive a skewed clock signal and to locally derive non-overlapping clock phases from the skewed clock signal.. Número de registro: **US 11/097,514. Patente invención**. Fecha de registro: 01/04/2005. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: Cadence Design Systems.

Cortadella, J.; Kondratyev, A.; Lavagno, L.; Sotiriou, C. P. **Asynchronous, multi-rail, asymmetric-phase, static digital logic with completion detection and method for designing the same**. Breve descripción: A method of converting a Boolean logic circuit into an asynchronous multi-rail circuit is provided. A Boolean logic circuit is converted into a first multi-rail circuit using at least Shannon's expansion. The first multi-rail circuit is technology mapped into a second multi-rail circuit. Completion detection circuitry is added which receives the primary outputs of the second multi-rail circuit.. Número de registro: **US 11/976,522. Patente invención**. Fecha de registro: 12/01/2005. País de registro: Estados Unidos de América. Ámbito: Internacional. Entidad titular: Foundation for Research and Technology (FORTH).

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## C.5 Software

Roig, O.; Cortadella, J.; Pastor, E. **VERSIFY**. Lenguaje de programación: C. Plataforma que lo soporta: UNIX. 1995.

Cortadella, J. **PETRIFY**. Lenguaje de programación: C. Plataforma que lo soporta: ESTACIO DE TREBALL AMB UNIX. 1995.

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## D. Productos

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### D.1 Datasets

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## E. Comisiones y sociedades

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### E.1 Pertenencia a comisión consultora o evaluadora

Vocal. Comitè d'Ètica de la UPC. 07/06/2021

Vocal. AQU. Comissió d'Avaluació de la Recerca. 01/04/2016

Vocal. Workshop on design Technologies. Definició de temes d'interés a l'àrea de "Technologies for Components and Subsystems". ESPRIT. 01/09/1996 - 01/09/1996.

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**Vocal. Comissió d'experts per a l'avaluació de projectes.** CICYT. 01/01/1996 - 31/12/1996.

**Vocal. Avaluació de projectes ESPRIT de "Long-Term Research".** ESPRIT. 01/01/1994

**Otros. Comision Interministerial de Ciencia y Tecnologia.** Agencia Nacional de Evaluación y Prospectiva.  
01/01/1992

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## **E.2 Pertenencia a tribunal o jurado de premio**

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## **E.3 Pertenencia a tribunal o jurado de concurso**

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## **E.4 Pertenencia a sociedad científica**

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**Miembro. Academia Europaea.** 01/01/2013

**Miembro. Institute of Electrical and Electronics Engineers (IEEE) - Fellow member.** 01/07/1987

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## **F. Colaboración en publicaciones y tesis**

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### **F.1 Colaboración en revista**

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### **F.2 Colaboración en libro**

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**Editor. *Applications and Theory of Petri Nets 2004, 25th International Conference, ICATPN 2004: Bologna, Italy, June 21-25, 2004: proceedings.*** Springer. 2004. ISBN: 978-3-540-27793-4.  
<<https://doi.org/10.1007/b98283>>

**Editor. *Concurrency and hardware design: advances in Petri nets.*** Springer. 2002. ISBN: 978-3-540-36190-9.  
<<https://doi.org/10.1007/3-540-36190-1>>