Curriculum Vitae de Antonio González

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1. Resumen

Antonio González se doctoró en la Universitat Politècnica de Catalunya (UPC), en Barcelona, España, en 1989. Se incorporó al Departamento de Arquitectura de Computadores de la UPC en 1986 y fue nombrado Catedrático en 2002. Creó y ha dirigido el grupo de investigación ARCO desde 1990. Fue el director fundador del Intel Barcelona Research Center de 2002 a 2014.

Sus investigaciones se han centrado en arquitectura de computadores, compiladores y procesamiento paralelo, con especial énfasis en microarquitectura de procesadores y generación de código. Ha publicado más de 400 artículos, ha dado más de 130 conferencias como invitado, es titular de 53 patentes y ha dirigido 42 tesis doctorales en estas áreas. Su índice H basado en Google Scholar es de 61.

Antonio ha sido investigador principal de 33 proyectos de investigación y ha recibido una subvención ERC Advanced Grant. Tiene un largo historial de innovaciones mediante transferencias tecnológicas de los resultados de sus investigaciones a productos comerciales, especialmente microprocesadores y sistemas informáticos en general.

Antonio ha sido presidente del programa de ICS 2003, ISPASS 2003, MICRO 2004, HPCA 2008 e ISCA 2011, y presidente general de MICRO 2008 y HPCA 2016, entre otros simposios. Ha formado parte de los comités de programa de más de 140 simposios internacionales en el campo de la arquitectura de computadores, incluidos ISCA, MICRO, HPCA, ASPLOS, PACT, ICS, ICCD, ISPASS, CASES e IPDPS. Ha sido editor asociado de IEEE Computer Architecture Letters, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Architecture and Code Optimization, ACM Transactions on Parallel Computing y Journal of Embedded Computing.

Entre los galardones de Antonio se incluyen el premio al mejor estudiante de ingeniería informática de España graduado en 1986, el premio Rosina Ribalta 2001 como director del mejor proyecto de doctorado en Tecnologías de la Información y las Comunicaciones, el premio Duran Farell 2008 a la investigación en tecnología, el Premio Nacional Aritmel de Informática 2009 al Ingeniero Informático del Año, el "Premio Rey Jaime I" 2013 en el área de Nuevas Tecnologías, y los Premios ICREA Academia 2014 y 2019. Fue incluido en el "IEEE/ACM MICRO Hall of Fame" en 2000, en el "IEEE HPCA Hall of Fame" en 2005 y en el "ACM/IEEE ISCA Hall of Fame" en 2013. Antonio es Fellow del IEEE y la ACM.

2. Información Personal

Apellido, nombre:	González, Antonio
Cargo actual:	Catedrático de Universidad), desde 2002
Universidad:	Universitat Politècnica de Catalunya
Departmento:	Arquitectura de Computadores
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3. Formación

- Doctor en Informática, Universitat Politècnica de Catalunya - Barcelona, Mayo 1989. Título: "Instruction Unit for Parallel Execution of Branches". Calificación: Cum Laude.
- Licenciado en Informática, Universitat Politècnica de Catalunya - Barcelona, Junio 1986. Premio al mejor estudiante de Ingeniería Informática de España graduado en 1986.

4. Expericia Profesional

- Profesor de Arquitectura de Computadores de la Universitat Politècnica de Catalunya (oct. 86 - actualidad). Profesor Titular desde 1990. Catedrático de Universidad desde 2002.
- Intel Barcelona Research Center (febrero de 2002 - mayo de 2014). Director.
- Departamento de Teledetección del Centre de Càlcul de la Universitat Politècnica de Catalunya (Sept. 84 - Sept- 86). Investigador asociado en el área de procesamiento digital de imágenes.

5. Publicaciones

5.1. Revistas

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[S.285] A. González and J. Tubella, "The Multipath Parallel Execution Model for Prolog", *Proc. of the 1st Int. Symposium on Parallel Symbolic Computation*, World Scientific Publishing (ISBN 981-02-2040-5), Linz (Austria), Sept. 1994, pp. 164-173.

[S.286] J. Tubella and A. González, "Combining Depth-first and Breadth-First Search in Prolog Execution", *Proc. of the Joint Conference on Declarative Programming,* (Dep. Legal V-2559-1994), Peñíscola (Spain), volume II, , Sept. 1994, pp. 452-454.

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[S.289] A. González, M. Valero, "The Xor Embedding: An Embedding of Hypercubes onto Rings and Toruses", *Proc. of the 1993 International Conference on Application-Specific Array Processors*, IEEE Computer Society Press (ISSN 1063-6862, ISBN 0-8186-3492-8), Venice (Italy), Oct. 1993, pp. 15-28.

[S.290] J. Tubella and A. González, "MEM: A New Execution Model for Prolog", *Proc. of the 19th. Euromicro Conference*, North Holland (ISSN 0165-6074), Barcelona (Spain), Sept. 1993, pp. 83-86.

[S.291] J. Tubella, A. González, "Measuring Scheduling Policies in Pure OR-Parallel Programs", *Proc. of the 1993 Congreso sobre Programación Declarativa, ProDe'93* (ISBN 84-00-07383-5), Blanes (Spain), Sept. 1993, pp. 57-71.

[S.292] M. Valero-García, A. González, "FFT for Massively Parallel Processors", *Proc. of the COST 229 WG4 Workshop on Massively Parallel Computing*, Madeira (Portugal), April 1993, pp. 83-94.

[S.293] A. González, J. Tubella y C. Aliagas, "An Evaluation Tool for the EDS Parallel Logic Programming System", *Proc. of the European Workshop on Parallel Computing*, IOS Press (ISBN 90-5199-080-4), Barcelona (Spain), March 1992, pp.566-569.

[S.294] J. Tubella, A. González y C. Aliagas, "Design and Evaluation of a Two-level Hierarchical Multiprocessor for Logic Programming", *Proc. of the tenth IASTED International Symposium on Applied Informatics*, Acta Press (ISBN 3-7153-0001-9), Innsbruck (Austria), Feb. 1992, pp.45-48.

[S.295] J. Tubella, A. González y C. Aliagas, "Representación de la carga de programas lógicos en la evaluación de un sistema multiprocesador", *Proc. of the Jornadas sobre Programación Declarativa*, Torremolinos (Málaga), Oct. 1991, pp. 497-518.

[S.296] A. González y J.M. Llabería "Instruction Fetch Unit for Parallel Execution of Branch Instructions", *Proc. of the 3rd. ACM International Conference on Supercomputing*, ACM Press (ISBN 0-89791-309-4), Heraklion (Greece), June 1989, pp. 417-426.

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[S.298] A. González, J.M. Llabería y J. Cortadella, "Zero-Delay Cost Branches in RISC Architectures", *Proc. of the IASTED International Symposium on Applied Informatics*, Acta Press (ISBN 0-88986-097-1), Grinderwald (Switzerland), Feb. 1988, pp. 24-27.

[S.299] A. González y J. Navarro, "Identificación Automática de vehículos", *Proc. of the II Jornadas del Grupo Técnico de Reconocimiento de Formas* (Dep. Legal M-32078-1986), Madrid (Spain), Oct 1986, p. 69.

5.3. Presentaciones en Simposios con Revision sin Actas

[W.1] P.H.E. Becker, J.-M. Arnau and A. González, "Boosting Point Cloud Search with a Vector Unit", *2nd Workshop on Robotics Acceleration with Computing Hardware, held in conjunction with the 56th IEEE/ACM International Symposium on Microarchitecture,* Toronto (Canada), Oct. 28, 2023.

[W.2] R. Huerta, M. Abaie-Shoushtary and A. González, "Analyzing and Improving Hardware Modeling of Accel-Sim", *1st Workshop on Computer Architecture Modeling and Simulation, held in conjunction with held in conjunction with the 56th IEEE/ACM International Symposium on Microarchitecture*, Toronto (Canada), Oct. 28, 2023.

[W.3] J. Cano, R. Kumar, A. Brankovic, D. Pavlou, K. Stavrou, E. Gibert, A. Martínez and A. González, "HW/SW Co-Designed Processors: Challenges, Design Choices and a Simulation Infrastructure for Evaluation", *ARM Research Summit,* Cambridge (UK), Sept. 11-13, 2017. Poster

[W.4] M. Anglada, R. Canal, J.L. Aragón and A. González, "Soft Error Rate Estimation for Combinational Circuits", *XXXI Conference on Design of Circuits and Integrated System*, Granada (Spain), Nov. 23-25, 2016.

[W.5] M. Riera, R. Canal, A. González, J. Abella, M. Anglada and M. Torrents, "Soft-Error Vulnerability Evolution: A 4D Study (Bulk/SOI, Planar/FinFET)", *International Workshop on Reliability and Aging in Forthcoming Electronic Systems, held in conjunction with IEEE European Test Symposium,* Cluj-Napoca (Romania), May 28-29, 2015.

[W.6] A. Brankovic, K. Stavrou, E. Gibert and A. González, "Analysis of CPI Variance for Dynamic Binary Translators/Optimizers Modules", *Workshop on Architectural and Microarchitectural Support for Binary Translation (AMAS-BT), held in conjunction with the 39th Int'l Symposium on Computer Architecture*, Portland, OR (USA), June 10, 2012.

[W.7] R. Kumar, A. Martínez and A. González, **"**Speculative Dynamic Vectorization to Assist Static Vectorization in a HW/SW Co-Designed Environment", *Compiler, Architecture and Tools Conference,* Intel Development Center, Haifa, (Israel), November 18 – 19, 2013. Poster

[W.8] Q. Cai, J. M. Codina, D. Ditzel, E. Gibert, F. Latorre, P. López, C. Madriles, G. Magklis, P. Marcuello, A. Martínez, R. Martínez, J. Sánchez, K. Stavrou and A. González, "Experiences with a HW/SW Co-Designed Architecture", *Intel Micro Architecture Conference*, Portland, OR (USA), June 4-5, 2009.

[W.9] G. Magklis, P. Marcuello, J. Sánchez, J. M. Codina, E. Gibert, F. Latorre, P. López, A. Piñeiro, J. González and A. González, "A P54C-Based FPGA Prototype with Dynamic Binary Optimization Support", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 4-7, 2008.

[W.10] J. Abella, P. Chaparro, X. Vera, J. Carretero and A. González, "Enabling High Frequency Register Files at Low Vcc Operation", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 4-7, 2008.

[W.11] J. Carretero, P. Chaparro, J. Abella, X. Vera and A. González, "Reliable Scheduler Control Logic Using Light-Weight Continuous Self Test", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 4-7, 2008.

[W.12] J. M. Codina, E. Gibert, F. Latorre, C. Madriles, G. Magklis, P. Marcuello, A. Martínez, R. Martínez, J. Sánchez and A. González, "Thalia: Hardware/Software Co-Design for Tera-Scale Processors", *6th Annual Research at Intel Day*, Santa Clara, CA (USA), June 11, 2008. Poster

[W.13] Q. Cai, J. González, P. Chaparro, G. Magklis and Al González, "Meeting Point Thread Characterization and its Applications", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 13-16, 2007.

[W.14] J. Abella, X. Vera and A. González, "Mechanisms to Mitigate NBTI-Related Aging", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 13-16, 2007.

[W.15] J.M. Codina, E. Gibert, F. Latorre, P. López, A. Piñeiro, J. Sánchez, C. Madriles, P. Marcuello, G. Magklis and A. González, "Thalia Technology: Software Dynamically-Scheduled Processors for Tera-scale Platforms", *Intel Systems Software Conference*, Santa Fe, NM (USA), May 30-31, 2007.

[W.16] J. González, Q. Cai, P. Chaparro, G. Magklis and A. González, "Thin-Film Thermo Electric Cooling-Based Dynamic Thermal Management", *Intel Power Conference*, Santa Fe, NM (USA), Dec. 14-15, 2006.

[W.17] J. González, P. Chaparro, G. Chrysler, G. Magklis, Q. Cai and A. González, "Building an Energy-Efficient Multi-Core Processor through Thread Fussion and Thread Delaying", *Intel Power Conference*, Santa Fe, NM (USA), Dec. 14-15, 2006.

[W.18] J. M. Codina, E. Gibert, F. Latorre, P. López, A. Piñeiro and A. González, "Thalia Technology: Software Dynamically-Scheduled Processors for Tera-scale Platforms", *3rd Annual Intel Platform Architecture Conference (IPAC)*, Santa Fe, NM (USA), Dec. 12-13, 2006.

[W.19] Q. Cai, P. Chaparro, G. Magklis, J. González and A. González, "Fused Threads", *2nd Workshop on MicroGrids*, Hitchin, Hertfordshire (UK), Dec. 4-5, 2006.

[W.20] G. Magklis, P. Chaparro, J. González and A. González, "Fine-Grain Power and Thermal Control with GALS Microarchitecture", *Intel Design and Test Technology Conference*, Portland, OR (USA), August 28-31, 2006.

[W.21] P. Chaparro, J. González, F. Latorre, G. Magklis and A. González, "An Integrated Physical Model for Microarchitectures", *Second Simulation Technology Summit (Simulation Extravaganza)*, Barcelona (Spain), Nov. 9-11, 2005.

[W.22] E. Gibert, F. Latorre, A. Piñeiro, J.M. Codina, J. González and A. González, "Implementation of a x86 Co-Designed Virtual Machine", *Second Simulation Technology Summit (Simulation Extravaganza)*, Barcelona (Spain), Nov. 9-11, 2005.

[W.23] A. Piñeiro, F. Latorre, P. Chaparro, J. González, E. Gibert, J.M. Codina and A. González, "Configurable Multi-Core Infrastructure Using ASIM", *Second Simulation Technology Summit (Simulation Extravaganza)*, Barcelona (Spain), Nov. 9-11, 2005.

[W.24] J. González, P. Chaparro, G. Magklis and A. González, "Low Power Clustered Microarchitecture", *Intel Power, Thermal, Acoustics and Energy Management Technology Pipeline Review*, Hillsboro, OR (USA), November 2-3, 2005.

[W.25] G. Magklis, J. González, P. Chaparro and A. González, "Fine-Grain Dynamic Voltage Scaling", *Intel Power, Thermal, Acoustics and Energy Management Technology Pipeline Review*, Hillsboro, OR (USA), November 2-3, 2005.

[W.26] Z. Sperber, L. Rappoport, A. González, A. Grandstein, Y. Almog, B. Valentine, D. Orenstein, J. Sebot, O. Golz, P. Chaparro, P. González, F. Latorre and A. Yoaz, "Power Efficient Clustered Micro-architecture", *4th Annual Intel Micro-architecture Conference*, Stevenson, WA (USA), June 2-3, 2005.

[W.27] C. García Quiñones, A. González, C. Madriles, P. Marcuello and J. Sánchez, "Speculative Multithreading for Next Generation Multi-Core Processors", *4th Annual Intel Micro-architecture Conference*, Stevenson, WA (USA), June 2-3, 2005.

[W.28] J. Sánchez, C. García, C. Madriles, P. Rundberg and A. González, "A Profile-Guided Tool to Extract Speculative Threads from Sequential Programs", *First Intel Dynamic Compilation and Profile-guided Optimization Conference*, Hillsboro, OR (USA), Nov. 20-21, 2003.

[W.29] P. Marcuello, A. González, "Exploiting Multithreading through Control and Data Dependence Speculation", *4th Int. Conf. on High Performance Computing*, Bangalore (India), Dec. 18-21, 1997.

[W.30] E. Ayguadé, C. Barrado, A. González, J. Labarta, J. Llosa, D. López, S. Moreno, D. Padua, F. Reig and M. Valero, "ICTINEO: A Tool for Research on ILP", *International Conference on High Performance Computing and Communications*, Pittsburgh, Pennsylvania (USA), Nov. 1996. Poster

5.4. Libros y Capítulos de Libros

[B.1] P.H.E. Becker, J.-M. Arnau and A. González, “Characterizing Self-Driving Tasks in General-Purpose Architectures”, *Advanced Computer Architecture and Compilation for High-performance Embedded Systems*, HiPEAC (ISBN 978-88-905806-8-0), pp. 117-120, 2021.

[B.2] A. González, “Trends in Processor Architecture”, *Harnessing Performance Variability in Embedded and High Performance Many/Multi-Core Platforms – A Cross-Layer Approach*, W. Fornaciari and D. Soudris editors, Springer (ISBN 978-3-319-91961-4), pp. 23-42, 2019.

[B.3] A. González, F. Latorre and G. Magklis, *Processor Microarchitecture. An Implementation Approach*, Morgan & Claypool Publishers (ISBN: 9781608454525, 9781608454532, ISSN: 1935-3235, 1935-3243), 2011.

[B.4] Y. Sazeides, P. Marcuello, J. Smith and A. González, “Data Speculation”, *Speculative Execution in High Performance Computer Architectures*, D. Kaeli and P. Yew editors, CRC Press (ISBN 1-58488-447-9), pp. 215-244, November 2005.

[B.5] P. Marcuello, J. Sánchez and A. González, “Multithreading and Speculation”, *Speculative Execution in High Performance Computer Architectures*, D. Kaeli and P. Yew editors, CRC Press (ISBN 1-58488-447-9), pp. 333-354, November 2005.

[B.6] D. Royo, M. Valero-García and Antonio González, “A New Jacobi Ordering for Multi-Port Hypercubes”, *Parallel Numerical Computations with Appications*, Kluwer Academic Publishers (ISBN 0-7923-8588-8), pp. 77-88, Sept. 1999.

[B.7] A. González and J. Tubella, "The Multipath Parallel Execution Model for Prolog", *Lecture Notes Series on Computing, Vol 5: Parallel Symbolic Computation*, World Scientific Publishing (ISBN 981-02-2040-5), pp. 164-173, Sept. 1994.

[B.8] A. González, J. Tubella y C. Aliagas, "An Evaluation Tool for the EDS Parallel Logic Programming System", *Parallel Computing: From Theory to Sound Practice*, W. Joosen and Elie Milgrom, editors, IOS Press (ISBN 90 5199 080 4), pp.566-569, March 1992.

6. Conferencias Magistrales e Invitadas

[K.1] A. González, "Energy-Efficient Architectures for Real-Time Rendering", *32nd International Conference on Parallel Architectures and Compilation Techniques*, Vienna (Austria), October 24, 2023. **Keynote.**

[K.2] A. González, "Removing Ineffectual Computations in Neural Networks", *Workshop on Accelerated Machine Learning, held in conjunction with 47th International Symposium on Computer Architecture*, Valencia (Spain), May 31, 2020. **Invited Talk.**

[K.3] A. González, "Milliwatt Human-Quality Speech Recognition", *1st Workshop on Emerging Deep Learning Accelerators, held in conjunction with High Performance Embedded Architectures and Compilers (HiPEAC) conference,* Valencia (Spain), January 21, 2019. **Keynote**

[K.4] A. González, "Domain-Specific Architectures: The Next Wave of Computing Innovation", *8th Workshop on Architectures and Systems for Big Data, held in conjunction with 45th International Symposium on Computer Architecture*, Los Angeles CA (USA), June 2, 2018. **Keynote**

[K.5] A. González, "The Unrealized Potential of Data Value Speculation", *Workshop on Negative Outcomes, Post-mortems, and Experiences, held in conjunction with the 49th Annual IEEE/ACM International Symposium on Microarchitecture,* Taipei (Taiwan), October 15, 2016. **Invited Talk**

[K.6] A. González, "The Revolution of Intelligent Devices", *Sensors to Cloud Architectures Workshop, held in conjunction with 22nd IEEE Symposium on High Performance Computer Architecture*, Barcelona (Spain), March 13, 2016. **Keynote**

[K.7] A. González, "The Next Revolution in Computing", *Compiler, Architecture and Tools Conference,* Intel Development Center, Haifa, Israel, November 18 – 19, 2013. **Keynote**

[K.8] A. González, "Computing Devices for the 20s", *Intel European Research and Innovation Conference*, Nice (France), October 22-23, 2013. **Invited Talk**

[K.9] A. González, "Los Nuevos Doctorados en el Ámbito de La Ingeniería Informática", *CEDI2013, IV Congreso Español de Informática*, Madrid (Spain), September 17-20, 2013. **Invited Round Table**

[K.10] A. González, "Research Strategy", *Intel EMEA Technology Conference*, Cambridge (UK), September 16-18, 2013. **Invited Panel**

[K.11] A. González, "Resilient Architectures for Energy Efficiency", *Euromicro DSD/SEEA Conferences*, Santander (Spain), Sept. 4-6, 2013. **Keynote**

[K.12] A. González, "Moore's Law Implications on Exascale Computing", *Intel Exascale Leadership Conference*, Geneva (Switzerland), May 18, 2011. **Invited Talk**

[K.13] A. González, "Moore's Law Implications in Energy Reduction", *6th Int. Conference on High Performance Embedded Architectures and Compilers (HiPEAC)*, Heraklion (Greece), Jan. 24-26, 2011. **Keynote**

[K.14] A. González, "Scalable Multicore Processors", *Intel European Research and Innovation Conference,* Braunschweig (Germany), September 21-22, 2010. **Invited Talk**

[K.15] A. González, "Trends in Multicore Processors", *72nd EAGE Conference & Exhibition, Workshop on The Role of Supercomputing in Reshaping the Future of the Seismic Imaging Industry*, Barcelona (Spain), June 13-14, 2010. **Invited Talk**

[K.16] A. González, "Moon Run: A Hardware/Software Co-Designed Processor", *Intel EMEA Strategic Mini Conference*, Brussels (Belgium), May 4-6, 2010. **Invited Talk**

[K.17] A. González, "Innovation: The Key to Leadership and Growth", *Innovation for Business Excellence*, Barcelona (Spain), November 26-27, 2009. **Invited Talk**

[K.18] A. González, "Multicore Processors for the Next Decade", *3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects, held in conjunction with the 36th International Symposium on Computer Architecture)*, Austin, TX (USA), June 20, 2009. **Keynote**

[K.19] A. González, "Hardware/Software Co-designed Processors", *2nd Workshop on Architectural and Microarchitectural Support for Binary Translation, held in conjunction with the 36th International Symposium on Computer Architecture*, Austin, TX (USA), June 20, 2009. **Keynote**

[K.20] A. González, "Multicore is Necessary But Not Sufficient", *Workshop on Design, Architecture, and Simulation of Chip Multi-Processors, held in conjunction with the 41st Annual International Symposium on Microarchitecture*, Lake Como (Italy), November 9, 2008. **Keynote**

[K.21] J. Abella, J. Carretero, P. Chaparro, X. Vera and A. González, "Dynamic Errors: Symptoms and Solutions", *Euro-Par Conference*, Las Palmas de Gran Canaria, Canary Islands (Spain), August 26-29, 2008. **Invited Talk**

[K.22] A. González, "Elastic Parallel Architectures", *Euro-Par*, Las Palmas de Gran Canaria, Canary Islands (Spain), August 26-29, 2008. **Keynote**

[K.23] J.M. Codina, E. Gibert, F. Latorre, P. López and A. González, "Codesigned Virtual Machines: New Opportunities in Processor Architecture", *Intel 12th EMEA Academic Forum*, Budapest (Hungary), June 12-14, 2007. **Invited Talk**

[K.24] A. González, "Future Microprocessors. Quo Vadis?", *Forum of the Information Technologies*, Barcelona (Spain), March 14th, 2007. **Invited Talk**

[K.25] A. González, "Processor Reliability", *Workshop on Computer Architecture Research Directions, held in conjunction with the International Symposium on High-Performance Computer Architecture*, Phoenix, AZ (USA), Febr. 11th, 2007. **Invited Panel**

[K.26] A. González, "The Intel Core Microarchitecture and Multi-Core Roadmap", *Cluster 2006 Workshop, held in conjunction with the IEEE International Conference on Cluster Computing*, Barcelona (Spain), September 25-28, 2006. **Invited Talk**

[K.27] A. González, "Resilient Processors", *11th Intel Academic Forum*, Dublin (Ireland), May 30 and 31 - June 1, 2006. **Invited Talk**

[K.28] A. González, "Challenges and Opportunities of Multi-Core Processors", *IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips IX),* Yokohama (Japan), April 19-21, 2006. **Keynote**

[K.29] A. González, "Revitalizing Computer Architecture Research", *CRA Conference on Grand Research Challenges*, Monterey Bay, CA (USA), December 4-7, 2005. **Invited Panel**

[K.30] A. González, "The Right-Hand Turn to Multi-Core Processors", *International Conference on Parallel Computing*, Málaga (Spain), September 13-16, 2005. **Keynote**

[K.31] A. González, "Multi-Core Chips. The Next Wave of Processor Microarchitecture", *International Conference on Parallel Processing (ICPP 2005)*, Oslo (Norway), June 14-17, 2005. **Keynote**

[K.32] A. González, "What are the important research challenges in temperature-aware computer systems?", *2nd Workshop on Temperature-Aware Computer Systems (TACS-2), held in conjunction with ISCA-32*, Madison, WI (USA), June 5, 2005. **Invited Panel**

[K.33] A. González, "The Renaissance of Thread-Level Parallelism", *10th Intel Academic Forum*, Gdansk (Poland), May 18-20, 2005. **Invited Talk**

[K.34] A. González, "How to Keep High-Performance Processors on Moore's Curve", *European Workshop on High Performance Technical Computing*, Maffliers (France), Sept. 19-22, 2004. **Keynote**

[K.35] A. González, "Retos y oportunidades de la futura nanotecnología en el diseño de procesadores", *XV Jornadas de Paralelismo*, Almería (Spain), September 15, 2004. **Keynote**

[K.36] A. González, "Complexity-Effective Processors in the Nanotechnology Era", *Workshop on Complexity-Effective Design, held in conjunction with Int. Symposium on Computer Architecture*, Munich (Germany), June 20, 2004. **Keynote**

[K.37] A. González, "Thermal Issues for Temperature-Aware Computer Systems", *International Symposium on Computer Architecture*, Munich (Germany), June 19, 2004. **Invited Tutorial**

[K.38] A. González, "Bridging the Research Gap between Academy and Industry", *10th. Int. Symp. on High Performance Computer Architecture*, Madrid (Spain), Feb. 14-18, 2004. **Invited Panel**

[K.39] A. González, "Power – A Main Challenge for Future Microprocessors", *Fifth Annual Tel Seminar and Tekes/Berkeley Seminar*, Oulu (Finland), Aug. 28, 2003. **Invited Talk**

[K.40] A. González, "Beyond Superscalar: Speculative Multithreaded Processors", *7th Intel European Academic Forum,* Budapest (Hungary), Sept. 17-20, 2002. **Invited Talk**

[K.41] A. González, "Rebuttal to 'Evaluation of the Performance of Polynomial Set Index Functions'", *Workshop on Duplicating, Deconstructing and Debanking, held in conjunction with the International Symp. on Computer Architecture*, Anchorage, Alaska (USA), May 26, 2002. **Invited Talk**

[K.42] A. González, "Computer Performance Evaluation Techniques", *NSF Workshop on Computer Performance Evaluation*, Austin, TX (USA), Dec. 1-5, 2001. **Invited Panel**

[K.43] A. González, "Dynamic Program Partitioning Approaches for Clustered Microarchitectures", *MEDEA Workshop, held in conjunction with International Conference on Parallel Architectures and Compilation Techniques*, Barcelona (Spain), Sept. 8, 2001. **Keynote**

[K.44] A. González, "Ongoing Research on Microarchitecture and Code Generation at UPC", *6th Intel EMEA Academic Forum*, Istanbul (Turkey), Sept. 5-7, 2001. **Invited Talk**

[K.45] A. González, "Computación de Altas Prestaciones", *IX Jornadas de Paralelismo*, San Sebastián (Spain), Sept. 2-4, 2001. **Invited Talk**

[K.46] A. González, "Arquitectura de los Computadores del Futuro", *IV Workshop IBERCHIP*, Mar de Plata (Argentina), March 11-13, 1998. **Invited Talk**

[K.47] A. González, "Has Exploitable ILP Reached a Point of Diminishing Returns?", *4th Int. Conf. on High Performance Computing*, Bangalore (India), Dec. 18-21, 1997. **Invited Panel**

[K.48] A. González and M. Valero, "Novel Organizations for Cache Memories", *Infofest'97*, Budva (Yugoslavia), Sept. 1997. **Invited Talk**

[K.49] A. González, "Data Speculation for Multiscalar Processors", *Infofest'97*, Budva (Yugoslavia), Sept. 1997. **Invited Talk**

[K.50] A. González, "Parallel Processing at AEDIMA", *ERCIM PPN Workshop on Parallel Processing Network*, Heraklion (Greece), June 1994. **Invited Talk**

[K.51] A. González, "Microprocesadores actuales", *I Forum de Informática Universidad-Empresa*, Barcelona (Spain), May 1994. **Invited Talk**

7. Conferencias Invitadas en la Industria y el Mundo Académico

[I.1] Removing Ineffectual Computations in GPU Architectures for Real Time Rendering, Chalmers University of Technology, Göteborg (Sweden), June 14, 2024.

[I.2] The Road to Cognitive Computing Architecture, University of Murcia, Murcia (Spain), June 26, 2023.

[I.3] The Era of Domain-Specific Architectures, Ghent University, Ghent (Belgium), November 28, 2019.

[I.4] The Revolution of Domain-Specific Architectures, Huawei Strategy and Technology Workshop, Shenzhen (China), May 13-15, 2019.

[I.5] Low-Power Human-Quality Speech Recognition, Huawei Strategy and Technology Workshop, Shenzhen (China), May 13-15, 2019.

[I.6] A Case for Domain-Specific Architectures and its Application to Energy-Efficient Speech Recognition, University of Southern California, Los Angeles CA (USA), May 21, 2018.

[I.7] Smart Processors, Institute of Computing Technology, Chinese Academy of Sciences, Beijing (China), November 21, 2017.

[I.8] Energy-Efficient Architectures for Speech Recognition, Northeastern University, Boston (USA), September 28, 2016.

[I.9] Cognitive Computers: The Next Wave of Computing Innovation, Universidad Complutense de Madrid, Madrid (Spain), May 9, 2016

[I.10] Energy Efficient GPUs, Northeastern University, Boston (USA), Nov. 12, 2015

[I.11] Low Power Microarchitectures for Graphics, Harvard University, Cambridge (USA), Nov. 10, 2015

[I.12] Towards Intelligent and Ubiquitous Computing, Northeastern University, Boston (USA), May 9, 2014

[I.13] The Internet of Intelligent Things, Harvard University, Cambridge (USA), May 8, 2014

[I.14] Energy-Efficient Computing, University of Cyprus, Dec. 7th, 2012

[I.15] Processor Microarchitecture, 8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES), Fiuggi (Italy), July 8-14, 2012. Seminar.

[I.16] Less Energy is More Performance, EcoCloud Inaugural Annual Event, Lausanne (Switzerland), June 18, 2012

[I.17] The Microprocessors of the Future, Universitat Politècnica de Catalunya, Barcelona (Spain), December 16, 2011

[I.18] Energy-Efficiency: The Main Challenge for Future Microprocessors, Jornadas de Inauguración Masters TIC, Universidad de Granada (Spain), December 1, 2011

[I.19] Intel Labs: Inventing the Future of Computing, Universitat Politècnica de Catalunya, Barcelona (Spain), November 30, 2011

[I.20] The Microprocessors of the Future, Seminar Series on Innovation and Entrepreneurship, Universidad Politècnica de Catalunya (UPC), Barcelona (Spain), May 31, 2011

[I.21] Resilient Microarchitectures, Universidad Complutense de Madrid, May 13, 2011

[I.22] Power-Efficient Processors through Hardware/Software Co-Design, Universitat Autònoma de Barcelona, Bellaterra, Barcelona (Spain), February 25, 2011

[I.23] Main Challenges and Opportunities for Future Microprocessors, Intel Labs Europe Technical Talk Series, Broadcast to all Intel Labs in Europe, August 5, 2010

[I.24] Software to the Rescue of Power, University of Malaga (Spain), July 26, 2010

[I.25] Power-Efficient Processors through Hardware/Software Co-Design, University of California at Berkeley, CA (USA), July 15, 2010

[I.26] Presente y Futuro de los Sistemas de Computación, mesa redonda del Curso de Verano “Presente y Futuro de los Sistemas de Computación”, Universidad de Castilla-La Mancha, Albacete (Spain), June 21st-23rd, 2010

[I.27] Procesadores co-diseñados mediante hardware y software, Curso de Verano “Presente y Futuro de los Sistemas de Computación”, Universidad de Castilla-La Mancha, Albacete (Spain), June 21st-23rd, 2010

[I.28] Inventing the Future, Intel Expert Event, Universitat Politècnica de Catalunya, Barcelona (Spain), June 1st, 2010

[I.29] Software to the Rescue of Power, University of Virgina, Charlottesville, VA (USA), May 10th, 2010

[I.30] Reliability and Variability Challenges for Future Microprocessors, Universitat Autònoma de Barcelona, Bellaterra, Barcelona (Spain), February 26th, 2010

[I.31] Designing Tomorrow's Microprocessors, Universitat Politècnica de Catalunya, Barcelona (Spain), February 8th, 2010

[I.32] How to Keep Historical Microprocessor Performance Improvement Rates, Universitat Autònoma de Barcelona, Bellaterra (Barcelona), December 12, 2008

[I.33] Codesigned Virtual Machines: New Opportunities in Processor Architecture, Universidad de Santiago de Compostela (Spain), November 23, 2007

[I.34] Resilient Processors, Norwegian University of Science and Technology, Trondheim (Norway), May 2, 2007

[I.35] Resilient Processors, NXP Semiconductors, Eindhoven (The Netherlands), February 6, 2007

[I.36] A Resilient Multi-Core Platform for High Reliability and Improved Lifetime, Microsoft Research, Redmond, WA (USA), Janurary 26, 2007

[I.37] Procesadores Multi-Core: La Respuesta a los Nuevos Retos Tecnológicos, Universidad de Murcia (Spain), May 19, 2006

[I.38] The Multi-Core Approach to Keep Processors on Moore's Curve, University of Edinburgh (UK), March 16, 2006

[I.39] Threading Technologies for Multi-Core Processors, Apple, Cupertino, CA (USA), Sept. 27, 2005

[I.40] Imagine the Future: Intel R&D, Magic in Your Hands, Intel Science and Technology Seminar, Madrid (Spain), May 31, 2005.

[I.41] Challenges and Opportunities for Processor Design with Future Nanotechnology, Gdansk University of Technology, Gdansk (Poland), May 19, 2005

[I.42] Speculative Threading: The Renaissance of Thread-Level Parallelism, Intel's Fellows Forum 2004, Sedona, AZ (USA), Sept. 29-Oct. 1, 2004

[I.43] Procesadores actuales y futuros (Round Table), Cursos de Verano 2004 de la Universidad Complutense de Madrid, El Escorial (Spain), July 5-9, 2004

[I.44] Procesadores para la era de la nanotecnología, Cursos de Verano 2004 de la Universidad Complutense de Madrid, El Escorial (Spain), July 5-9, 2004

[I.45] Cómo seguir explotando la ley de Moore en futuros microprocesadores, Universidad de Castilla La Mancha, Albacete (Spain), May 25, 2004

[I.46] Compiler-Assisted Speculative Multithreading, Microprocessor Research Labs, Intel, Half Moon Bay - California (USA), February 13-14, 2003

[I.47] The Post-Superscalar Generation, Northeastern University, Boston (USA), December 6th, 2002

[I.48] New Challenges in Processor Microarchitecture, University of Pisa, Pisa (Italy), March 8, 2002

[I.49] Power-Effective Microarchitectures Through Clustering, Intel Corporation, Haifa (Israel), November 19, 2001

[I.50] Speculative Multithreaded Microarchitectures, Intel Corporation, Haifa (Israel), November 15, 2001

[I.51] Power-Effective Microarchitectures Through Clustering, Transmeta, Santa Clara - CA (SA), October 31, 2001

[I.52] Power-Effective Microarchitectures Through Clustering, Intel Corporation, Santa Clara - CA (USA), October 31, 2001

[I.53] The Post-Superscalar Era, University of Illinois at Urbana-Champaign (USA), October 29, 2001

[I.54] Clustered Microprocessors: A Power-Effective Microarchitecture, Intel Corporation, Hillsboro - OR (USA), October 23, 2001

[I.55] Clustered, Power-Aware, Speculative Multithreaded Processors, Intel Corporation, Austin - TX (USA), October 16, 2001

[I.56] The Post-Superscalar Era, University of Texas at Austin - TX (USA), October 15, 2001

[I.57] The Post-Superscalar Era, University of Wisconsin – Madison (USA), October 12, 2001

[I.58] The Post-Superscalar Era, Intel Corporation, Santa Clara - CA (USA), October 3, 2001

[I.59] Speculative Multithreaded Microarchitectures, Intel Corporation, Hillsboro - OR (USA), August 16, 2001.

[I.60] Speculative Multithreaded Microarchitecture, IBM Thomas J. Watson Research Center, Yorktown Heights - NY (USA), August 9, 2001

[I.61] Research Trends in Processor Microarchitecture, Intel Microprocessor Research Lab, Santa Clara - CA (USA), August 2, 2001

[I.62] Low Power Microarchitectures, Universitat Rovira I Virgili, Tarragona (Spain), May 29, 2001

[I.63] Clustered Microprocessors: A Power-Effective Microarchitecture, Philips Research Laboratories, Eindhoven (The Netherlands), April 11, 2001

[I.64] Processor Microarchitecture and Instruction Scheduling, Intel Microprocessor Research Lab, Santa Clara - CA (USA), December 13, 2000

[I.65] Fighting Wire Delays and Power Consumption: Clustered Micro-architectures, IBM Thomas J. Watson Research Center, Yorktown Heights - NY (USA), December 7, 2000

[I.66] Microarchitectural Support for Low Power, IBM Thomas J. Watson Research Center, Yorktown Heights - NY (USA), December 6, 2000

[I.67] Fighting Wire Delays: Clustered Microarchitectures, Universidad de Murcia (Spain), October 6, 2000

[I.68] Fighting Wire Delays: Clustered Microarchitectures, Universidad de Valencia (Spain), October 4, 2000

[I.69] Clustered Speculative Microarchitectures, University of Paris Sud, Paris (France), May 11, 2000

[I.70] Clustered Speculative Microarchitectures, Compaq Computer Co., Shrewsbury - MA (USA), January 2000

[I.71] Instruction Scheduling for Clustered Architectures, HP Labs, Boston (USA), January 2000

[I.72] Microarquitecturas Cluster para Procesadores, Universitat Rovira i Virgili, Tarragona (Spain), June 1999

[I.73] La Generación de Procesadores Post-Superscalar, Universitat Rovira i Virgili, Tarragona (Spain), June 1999

[I.74] Register File Architectures, Northwestern University – Chicago (USA), May 1999

[I.75] Clustered Microarchitectures, University of Minnesota – Minneapolis (USA), May 1999

[I.76] Register File Architectures, University of Madison – Wisconsin (USA), May 1999

[I.77] Clustered Microarchitectures, University of Madison – Wisconsin (USA), May 1999

[I.78] Multithreaded Decoupled Access Execute Processors, University of Edinburgh (UK), December 1998

[I.79] Clustered Speculative Multithreaded Architectures, University of Edinburgh (UK), December 1998

[I.80] Beyond Superscalar Processors, Universidad de Cantabria – Santander (Spain), May 1998

[I.81] Procesadores de Altas Prestaciones, Asociación de Técnicos de Informática (ATI), Madrid (Spain), June 1997

[I.82] Microarquitectura de los Procesadores Paralelos, Universidad de Alcalá de Henares (Spain), April 1997

[I.83] The Effectiveness of XOR-mapping schemes to eliminate cache conflict misses, University of Edinburgh (UK), August 1996

[I.84] Procesadores Superscalares, Universidad de Las Palmas de Gran Canaria (Spain), May 1996

[I.85] Procesadores Superscalares, Universidad de Málaga (Spain), March 1995

8. Director de Tesis Doctorales

[PhD.1] Raúl Taranco, "Architectural Strategies to Enhance the Latency and Energy Efficiency of Mobile Continuous Visual Localization Systems"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, August 29, 2024
Co-advisor: José María Arnau

[PhD.2] Diya Joseph, "Improving Memory Access Efficiency for Real-Time Rendering in Tile-Based GPU Architectures"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, July 26, 2024
Co-advisor: Juan Luis Aragón

[PhD.3] David Corbalán Navarro, "Diseño de GPUs Eficientes Energéticamente Explotando la Coherencia entre Fotogramas y Optimizando los Accesos a Memoria"
Universidad de Murcia
Qualification: Excellent Cum Laude, June 26, 2023
Co-advisor: Juan Luis Aragón

[PhD.4] Daniel Pinto, "Acceleration of Automatic Speech Recognition for Low-Power Devices"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, November 09, 2022
Co-advisor: José María Arnau

[PhD.5] Albert Segura, "High-Performance and Energy-Efficient Irregular Graph Processing on GPU Architectures"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, February 18, 2021
Co-advisor: José María Arnau

[PhD.6] Franyell Silfa, "Energy-Efficient Architectures for Recurrent Neural Networks"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, January 25, 2021
Co-advisor: José María Arnau

[PhD.7] Marc Riera, "Low-Power Accelerators for Cognitive Computing"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, October 9, 2020
Co-advisor: José María Arnau

[PhD.8] Martí Anglada, "Exploiting Frame Coherence in Real-Time Rendering for Energy-Efficient GPUs"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, June 9, 2020
Co-advisor: Joan Manuel Parcerisa

[PhD.9] Reza Yazdani, "Ultra Low-Power, High-Performance Accelerator for Speech Recognition"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, July 25, 2019
Co-advisor: José María Arnau

[PhD.10] Hamid Tabani, "Low-Power Architectures for Automatic Speech Recognition"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, February 21, 2018
Co-advisors: José María Arnau and Jordi Tubella

[PhD.11] Sudhanshu Shekhar Jha, "Power-Constrained Aware and Latency-Aware Microarchitectural Optimizations in Many-Core Processors"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, October 5, 2016
Co-advisors: Ayose Falcón and Jordi Tubella

[PhD.12] Gem Dot, "Co-designed Solutions for Overhead Removal in Dynamically Typed Languages"
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, July 27, 2016
Co-advisor: Alejandro Martínez

[PhD.13] Aleksandar Brankovic, “Performance Simulation Methodologies for Hardware/Software Co-Designed Processors”
Universitat Politècnica de Catalunya (UPC)
Qualification: Excellent Cum Laude, March 17, 2015
Co-advisors: Kyriakos Stavrou and Enric Gibert

[PhD.14] Rakesh Kumar, “Optimizing SIMD Execution on Hw/Sw Co-Designed Processors”
Universitat Politècnica de Catalunya (UPC)
Qualification: Excelente, July 24, 2014
Co-advisor: Alejandro Martínez

[PhD.15] Shrikanth Ganapathy, “Reliability in the face of Variability in Nanometer Embedded Memories”
Universitat Politècnica de Catalunya (UPC)
Qualification: Excelente – Cum Laude, April 28th, 2014
Co-advisor: Ramon Canal and Antonio Rubio

[PhD.16] Pedro López, “Efficient Hardware/Software Co-Designed Schemes for Low-Power Processors”
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, March 17th, 2014
Co-advisor: Fernando Latorre and Enric Gibert

[PhD.17] Stefan Bieschewski, “Design of a Distributed Memory Unit for Clustered Microarchitectures”
Universitat Politècnica de Catalunya (UPC)
Qualification: Apto, June 20th, 2013
Co-advisor: Joan Manuel Parcerisa

[PhD.18] Govind Sreekar Shenoy, “Architecture Support for Intrusion Detection Systems”
Universitat Politècnica de Catalunya (UPC)
Qualification: Apto, October 30th, 2012
Co-advisor: Jordi Tubella

[PhD.19] Carlos Madriles, “Mitosis Based Speculative Multithreaded Architectures”
Universitat Politècnica de Catalunya (UPC)
Qualification: Apto – Cum Laude, July 23rd, 2012
Co-advisors: Josep M. Codina and Pedro Marcuello

[PhD.20] Abhishek Deb, “HW/SW Mechanisms for Instruction Fusion, Issue and Commit in Modern Microprocessors”
Universitat Politècnica de Catalunya (UPC)
Qualificacion: Apto, May 3rd, 2012
Co-advisor: Josep M Codina

[PhD.21] Indu Bhagat, “Code Optimizations for Narrow Bitwidth Architectures”
Universitat Politècnica de Catalunya (UPC)
Qualification: Apto – Cum Laude, February 23rd, 2012
Co-advisors: Enric Gibert and Jesús Sánchez.

[PhD.22] Marc Lupon, “Architectural Support for High-Performance Hardware Transactional Memory Systems”
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, December 23rd, 2011
Co-advisor: Grigorios Magklis

[PhD.23] Javier Lira, “Managing Dynamic Non-Uniform Cache Architectures”
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, November 25th, 2011
Co-advisor: Carlos Molina
Recipient of the UPC PhD award (Premio extraordinario de doctorado de la UPC)

[PhD.24] Rakesh Ranjan, “Speeding up Sequential Applications on Multicore Platforms”,
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, November 11th, 2010
Co-advisors: Fernando Latorre, Pedro Marcuello

[PhD.25] Alex Aletà, “Instruction Scheduling for Clustered Processors Based on Graph Techniques”,
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, October 15th, 2009
Co-advisor: Josep M. Codina

[PhD.26] Fernando Latorre, “Clustered Multithreaded Processors”,
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, June 18th, 2009
Co-advisor: José González

[PhD.27] Eduardo Quiñones , “Predicated Execution and Register Windows for Out-of-Order Processors”,
Universitat Politècnica de Catalunya (UPC)
Qualification: Sobresaliente – Cum Laude, November 18th, 2008
Co-advisor: Joan M. Parcerisa

[PhD.28] Josep Maria Codina, “Single-Phase Instruction Scheduling for Clustered Architectures”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, April 14th, 2008
Co-Advisor: Jesús Sánchez

[PhD.29] Pedro Chaparro, “Thermal-Aware Microarchitectures”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, Feb. 17th, 2008
Co-Advisor: José González

[PhD.30] Carlos Molina, “Microarchitectural Techniques to Exploit Repetitive Computations and Values”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, Dec 14th, 2005
Co-Advisor: Jordi Tubella

[PhD.31] Álex Pajuelo, “Speculative Vectorization for Superscalar Processors”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, Nov 24th, 2005
Co-Advisor: Mateo Valero

[PhD.32] Enric Gibert, “Clustered Data Cache Designs for VLIW Processors”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, Nov 16th, 2005
Co-Advisor: Jesús Sánchez

[PhD.33] Jaume Abella, “Adaptive and Low-Complexity Microarchitectures for Power Reduction”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, July 19th, 2005
Recipient of the UPC PhD award (Premio extraordinario de doctorado de la UPC)

[PhD.34] Joan Manuel Parcerisa, “Design of Clustered Superscalar Microarchitectures”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, June 17th, 2004

[PhD.35] Ramon Canal, "Power- and Performance- Aware Architectures”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, June 14th, 2004
Co-Advisor: James E. Smith

[PhD.36] Pedro Marcuello Pascual, “Speculative Multithreaded Processors”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, July 22nd, 2003

[PhD.37] Teresa Monreal Arnal, “Técnicas Hardware para Optimizar el Uso de los Registros en Procesadores Superscalares”,
Universidad de Zaragoza
Qualification: sobresaliente - Cum Laude, June 17th, 2003
Co-Advisor: Mateo Valero and Víctor Viñals

[PhD.38] Juan Luis Aragón Alcaraz, “Reducción de la Penalización de los Saltos Condicionales Mediante Estimación de Confianza”,
Universidad de Murcia
Qualification: sobresaliente - Cum Laude, February 25th, 2003
Co-Advisor: José González

[PhD.39] Jesús Sánchez, “Smart Memory Management Through Locality Analysis”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, November 6th, 2001

[PhD.40] José González, “Speculative Execution Through Value Prediction”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, January 18th, 2000

[PhD.41] Luis Díaz de Cerio, “CALMANT: Un método sistemático para la ejecución de algoritmos con topología hipercubo en mallas y toros”,
Universitat Politècnica de Catalunya (UPC)
Qualification: sobresaliente - Cum Laude, December 14th, 1998
Co-Advisor: Miguel Valero

[PhD.42] Jordi Tubella, “Multipath: Un sistema para la programación lógica”,
Universitat Politècnica de Catalunya (UPC)
Qualification: Apto - Cum Laude, November 13th, 1996

9. Participación en Proyectos de I+D

9.1. Investigador Principal

1. Grupo de Investigación Consolidado SGR-Cat (2021 SRG 00383, AGAUR-Generalitat de Catalunya), 2022-2024.
2. Domain-Specific Architectures for Energy-Efficient Computing Systems (PID2020-113172RB-I00, Spanish National Research Agency), 2021-2025.
3. CoCoUnit: An Energy-Efficient Unit for Cognitive Computing (ERC-ADG-2018 833057, ERC Advanced Grant, H2020), 2019-2024.
4. Intelligent, Ubiquitous and Energy-Efficient Computing Systems (TIN2016-75344-R, Spanish National Research Agency), 2016-2020.
5. Grupo de Investigación Consolidado (2017SGR11, AGAUR-Generalitat de Catalunya), 2017-2019
6. IEEE Simposio Internacional en Arquitecturas de Alto Rendimiento, (TIN2015-63344-CIN, Ministerio de Economía y Competitividad), 2015
7. Intel Barcelona Research Center (Intel), 2002-2014
8. Cross-Layer Early Reliability Evaluation for the Computing Continuum (EU FP7, project num. 611404), 2013-2016
9. Terascale Reliable Adaptive Memory Systems (EU FP7, project num. 248789), 2010-2013
10. Microarquitectura y Compiladores para Futuros Procesadores II (TIN2010-19368, Ministerio de Ciencia e Innovación), 2010-2013
11. Microarquitectura y Compiladores para Futuros Procesadores (TIN2007-61763, Ministerio de Educación y Ciencia), 2007-2010
12. Grupo de Investigación Consolidado (2005SGR00950, AGAUR-Generalitat de Catalunya), 2005-2007
13. Variations-Aware Circuit Designs for Microprocessors (Intel), 2005-2008
14. Microarquitectura y Compiladores para Futuras Nanotecnologías (TIN2004-03072, Ministerio de Educación y Ciencia), 2004-2007
15. Power and Communication-Aware Microarchitectures (Intel), 2003-2006
16. Memory Architecture and Compiler Support for Clustered EPIC Processors (Intel), 2003-2006
17. Low Power High Performance Microarchitecture and Compilation (GR/R40005, EPSRC-United Kingdom), 2002-2005
18. Adaptive Microarchitectures for Power Reduction (Intel), 2002-2005
19. A Networked Training Initiative for Embedded Systems Design - ANTITESYS (EU IST Program), 2002-2004
20. Customized Memory Architectures for Embedded Processors (STMicroelectronics), 2001-2004
21. Speculative Vector Processors (Intel), 2001-2004
22. Memory Architectures for Multithreaded Processors (Intel), 2001-2004
23. Register File Extensions for High Level Semantics (Intel), 2000-2003
24. Consultancy on Technologies for Compilers and Microprocessors (STMicroelectronics), 2000-2001
25. Instruction Scheduling Techniques for Clustered VLIW architectures (Analog Devices Inc.), 2000-2003
26. The Subscalar Microarchitecture: An Ultra-Low Power Architecture (IBM), 2000-2003
27. Compiler Scheduling Techniques for ADI Digital Signal Processor (Analog Devices Inc.), 1999-2000
28. Herramientas de Análisis y Optimización de la Jerarquía de Memoria (TIC98-1704-CE, CICYT), 1999-2000
29. Memory Hierarchy Analysis and Optimization Tools for the End-User (EU ESPRIT project 24942), 1997-2001
30. Coopernet (EU ALFA), 1996-1997

31. Sinergia entre compilador y arquitectura en la computación de altas prestaciones (Acciones Integradas, Ministerio de Educación y Ciencia), 1996-1997
32. Supercomputer Highly Parallel System Software - SHIPS Software (EU ESPRIT project 9601), 1994-1996
33. Supercomputer Highly Parallel System – SHIPS (EU ESPRIT project 6253), March 1994-1995
34. European Declarative System – EDS (EU ESPRIT project 2025), 1989-1992

9.2. Miembro del Consejo Científico Asesor

1. MANGO: Exploring Manycore Architectures for Next Generation HPC systems (EU H2020, project number 671668), 2015-2019

9.3. Investigador

1. Microarquitectura y Compiladores para Futuros Procesadores III (TIN2013-44375-R, Ministerio de Economía y Competitividad), 2014-2017
2. Grupo de Investigación Consolidado (2014SGR1205, AGAUR-Generalitat de Catalunya), 2014-2016
3. Grupo de Investigación Consolidado (2009SGR1250, AGAUR-Generalitat de Catalunya), 2009-2013
4. Computación de altas prestaciones III (TIC2001-0995, CICYT), 2001-2004
5. UPC-USA Universities Collaboration (Fulbright, Ministerio de Educación y Ciencia), 1999-2001
6. Grupo de Investigación Consolidado (1999SGR00128, AGAUR-Generalitat de Catalunya), 1999-2001
7. Computación de altas prestaciones II (TIC 98/0511-C02-01, CICYT), 1998-2001
8. Short and Long Term Optimization of Electricity Generation and Trading in a Competitive Energy Market – SLOEGAT (EU ESPRIT), 1996-1999
9. Grupo de Investigación Consolidado (1997SGR0005, AGAUR-Generalitat de Catalunya), 1997-1999
10. Parallelisation of the Chirp Scaling Algorithm SAR Processor - PARSAR (EU ESPRIT PCI-II), 1996-1997
11. Grupo de Investigación Consolidado (95-00402, AGAUR-Generalitat de Catalunya), 1995-1997
12. Computación de altas prestaciones (TIC 95/429, CICYT), 1995-1998
13. Performance-critical Applications of Parallel Architectures – APPARC (EU ESPRIT), 1992-1995
14. Grupo de Investigación Consolidado (93-QUA003, AGAUR-Generalitat de Catalunya), 1993-1995
15. Arquitecturas paralelas orientadas a aplicaciones simbólicas (TIC 91/1036, CICYT), 1992-1994
16. Supercomputer Highly Parallel System – SHIPS (EU ESPRIT project 6253), 1992-March 1994
17. Diseño y evaluación de arquitecturas orientadas a lenguajes de alto nivel (TIC 89/0300), 1989-1991
18. Diseño de Arquitecturas Paralelas de Alta Velocidad a Bajo Coste (PA85-0314, CAICYT), 1985-1989

10. Organización de Simposios

10.1. Presidente del Programa

1. Intel European Technology Conference (IETC), Brussels (Belgium), November 27-28, 2012
2. 38th International Symposium on Computer Architecture (ISCA), San Jose, CA (USA), June 4-8, 2011
3. IEEE International Parallel and Distributed Processing Symposium (IPDPS), Rome (Italy), May 25-29, 2009. Program Vice-Chair
4. The 14th International Symposium on High-Performance Computer Architecture (HPCA), Salt Lake City, UT (USA), February 16-20, 2008
5. 37th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Portland (USA), Dec. 4-8, 2004
6. 17th Annual ACM International Conference on Supercomputing (ICS), San Francisco, CA (USA), June 23-26, 2003
7. 2003 Int. Symp. on Performance Analysis of Systems and Software (ISPASS), Austin (USA), 2003
8. 6th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), held in conjunction with the 35th Int. Symposium on Microarchitecture (MICRO), Istanbul (Turkey), 2002
9. 5th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Austin (USA), 2001
10. Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC) in conjunction with the 33rd Int. Symposium on Microarchitecture, Monterrey (USA), 2000
11. Workshop on Computer Architecture Education, in conjunction with the 25th Int. Symposium on Computer Architecture, Barcelona (Spain), 1998
12. 3rd Euromicro Workshop on Parallel and Distributed Processing, San Remo (Italy), 1995

10.2. Presidente General

1. International Symposium on High-Performance Computer Architecture, Barcelona (Spain), March 12-16, 2016
2. 41st IEEE/ACM International Symposium on Microarchitecture, Lake Como, Italy, Nov. 8-12, 2008
3. 19th Euromicro Conference, Barcelona (Spain), 1993

10.3. Miembro del Comité Organizador

1. Industry Liaison Chair of the 47th International Symposium on Computer Architecture, Valencia (Spain), 2020.
2. Member of the Steering Committee of the Annual IEEE/ACM International Symposium on Microarchitecture since 2017.
3. Member of the Steering Committee of the International Symposium on Computer Architecture, from 2011 to 2013.
4. Member of the Steering Committee of the International Symposium on High-Performance Computer Architecture, from 2009 to 2011.
5. Member of the Steering Committee of the International Conference on Supercomputing, from 2003 to 2007
6. 10th Design, Automation and Test in Europe Conference (DATE 2007), Nice (France), April 16-20, 2007. **Co-organizer of the special session: "The ultimate microprocessor in 2020?"**
7. 8th Int. Symposium on High-Performance Computer Architecture (Workshop chair), Cambridge (USA), 2002
8. 25th. Int. Symp. on Computer Architecture (local chair for workshops and tutorials), Barcelona (Spain), 1998
9. Member of the Advisory Board of the Euro-Par Conference since 1995

10.4. Miembro del Comité del Programa

1. 51st International Symposium on Computer Architecture (ISCA), Tokyo (Japan), June 21-25, 2025.
2. 57th IEEE/ACM International Symposium on Microarchitecture (MICRO), Austin, TX (USA), Nov. 2-6, 2024.
3. 56th IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto (Canada), Oct. 28-Nov. 1, 2023.
4. 50th International Symposium on Computer Architecture (ISCA), Orlando, FL (USA), June 19-21, 2023.
5. 29th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Montreal (Canada), Feb. 25 – March 1, 2023.
6. 49th International Symposium on Computer Architecture (ISCA), New York, NY (USA), June 18-22, 2022
7. 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Athens, Greece, Oct. 16-20, 2021.
8. 48th International Symposium on Computer Architecture (ISCA), Valencia (Spain), May 22-26, 2021.
9. 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Seoul (South Korea), Feb. 27 – March 3, 2021.
10. 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO), Athens, Greece, Oct. 17-21, 2020.
11. 47th International Symposium on Computer Architecture (ISCA), Valencia (Spain), May 30-June 3, 2020.
12. 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA), San Diego, CA (USA), Feb. 22-26, 2020.
13. 52nd IEEE/ACM International Symposium on Microarchitecture (MICRO), Columbus, OH (USA), Oct. 12-16, 2019.
14. International Workshop on Exploitation of High Performance Heterogeneous Architectures and Accelerators, as part of 17th International Conference on High Performance Computing and Simulation, Dublin (Ireland), July 15-19, 2019.
15. 25th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Washington, DC (USA), Feb. 16-20, 2019.
16. 51st. Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Fukuoka City (Japan), Oct. 20-24, 2018.
17. 45th International Symposium on Computer Architecture (ISCA), Los Angeles, CA (US), June 1-6, 2018.
18. 24th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Vienna (Austria), Feb. 24-28, 2018.
19. 44th International Symposium on Computer Architecture (ISCA), Toronto (Canada), June 24-28, 2017.
20. 23rd. International Symposium on High-Performance Computer Architecture (HPCA), Austin TX (USA), Feb. 4-8, 2017.
21. 43rd. International Symposium on Computer Architecture (ISCA), Seoul (South Korea), June 18-22, 2016.
22. International Symposium on Code Generation and Optimization (CGO), Barcelona (Spain), March 12-18, 2016.
23. 2nd Workshop on Approximate Computing, in conjunction with HiPEAC Conference, Prague (Czech Republic), Jan. 20, 2016.
24. 27th International Symposium on Computer Architecture and High Performance Computing, Santa Catarina (Brazil), Oct. 18-21, 2015.
25. 1st International Workshop on High-Performance Interconnection Networks Towards the Exascale and Big-Data Era, in conjunction with IEEE Cluster Conference, Chicago IL (USA), Sept. 8, 2015.
26. 42nd International Symposium on Computer Architecture (ISCA), Portland OR (USA), June 13-17, 2015.
27. 1st International Workshop on Reliability and Aging in Forthcoming Electronic Systems, Cluj-Napoca (Romania), May 28-29, 2015.
28. 20th Int. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Istanbul (Turkey), March 14-18, 2015
29. The 21st IEEE International Symposium on High-Performance Computer Architecture (HPCA), USA, February 2015.

30. The 20th IEEE International Symposium on High Performance Computer Architecture (HPCA), collocated with PPoPP-2014 and CGO-2014, Orlando, FL (USA), February 15-19, 2014
31. The 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Davis, CA (USA), December 7-11, 2013
32. The 5th USENIX Workshop on Hot Topics in Parallelism (HotPar2013), San Jose, CA (USA), June 24-25, 2013
33. The 19th IEEE International Symposium on High Performance Computer Architecture, collocated with PPoPP-2013 and CGO-2013, Shenzhen (China), February 23-27, 2013
34. 39th Intl Symposium on Computer Architecture (ISCA), Portland, OR (USA), June 9-13, 2012
35. 44th IEEE/ACM International Symposium on Microarchitecture (MICRO), Porto Alegre (Brazil), December 3-7, 2011
36. The 15th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Newport Beach, CA (USA), March 5 - 11, 2011
37. The 17th International Symposium on High-Performance Computer Architecture (HPCA), San Antonio, TX (USA), February 12-16, 2011
38. The 37th ACM IEEE International Symposium on Computer Architecture (ISCA), Saint-Malo (France), June 19-23, 2010
39. International Conference on Compiler Construction, Paphos (Cyprus), March 20-28, 2010
40. The International Symposium on High-Performance Computer Architecture (HPCA), Bangalore (India), January 9-13, 2010
41. The 2nd Workshop on Architectural and Microarchitectural Support for Binary Translation (AMAS-BT), held in conjunction with the 36th Annual International Symposium on Computer Architecture (ISCA), Austin, TX (USA), June 20-24, 2009
42. The 36th Annual International Symposium on Computer Architecture (ISCA), Austin, TX (USA), June 20-24, 2009
43. The 15th International Symposium on High-Performance Computer Architecture (HPCA), Raleigh, NC (USA), February 14-18, 2009
44. The 15th Annual IEEE International Conference of High Performance Computing (HiPC 2008), Bangalore (India), December 17-20, 2008
45. Parallel Architectures and Compilations Techniques (PACT), Toronto (Canada), October 25-29, 2008
46. 11th Euromicro Conference on Digital System Design (DSD), Parma (Italy), September 3-5, 2008
47. The 35th Annual International Symposium on Computer Architecture (ISCA 2008), Beijing (China), June 21-25, 2008
48. 22nd ACM International Conference on Supercomputing (ICS), Island of Kos, Aegean See (Greece), June 7-12, 2008
49. The Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP), held in conjunction with the 40th Annual International Symposium on Microarchitecture (MICRO), Chicago, IL (USA), December 2, 2007
50. The 40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Chicago, IL (USA), December 1-5, 2007
51. The 2nd International Conference on Nano-Networks, Catania (Italy), September 24-26, 2007.
52. The 10th Euromicro Conference on Digital System Design (DSD), Lübeck (Germany), August 29-31, 2007
53. The 34th International Symposium on Computer Architecture (ISCA), San Diego, CA (USA), June 9-13, 2007
54. The 2007 International Symposium on Code Generation and Optimization (CGO), San Jose, CA (USA), March 11-14, 2007
55. Intel Power Conference, Inn and Spa at Loretto, Santa Fe, NM (USA), Dec. 14-15, 2006
56. Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP), held in conjunction with the 39th Annual International Symposium on Microarchitecture, Orlando, FL (USA), December 10, 2006
57. The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Orlando, FL (USA), December 9-13, 2006

58. 2006 IEEE International Symposium on Workload Characterization (IISWC), Hilton Hotel, San Jose, CA (USA), October 25-28, 2006
59. Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Hilton Hotel, San Jose, CA (USA), October 21, 2006
60. 1st International Conference on Nano-Networks (Nano-Net 2006), Lausanne (Switzerland), September 14-16, 2006
61. The 9th Euromicro Conference on Digital System Design (DSD), Conference Hotel Croatia, Cavtat (Croatia), August 30 - September 1, 2006
62. 7th Workshop on Complexity-Effective Design (WCED), Boston, MA (USA), June 18, 2006
63. 33rd Annual International Symposium on Computer Architecture (ISCA), Boston, MA (USA), June 17-21, 2006
64. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Austin, TX (USA), March 19-21, 2006
65. 12th Annual IEEE International Conference on High Performance Computing (HiPC), Goa, India, December 18-21, 2005
66. 1st Workshop on Architectural Reliability (WAR), held in conjunction with the 38th International Symposium on Microarchitecture (MICRO), New Hilton Diagonal Mar Hotel, Barcelona (Spain), Sunday, November 13th, 2005
67. IEEE International Symposium on Workload Characterization (IISWC), Crowne Plaza Austin Hotel, Austin, TX (USA), October 6-8, 2005
68. IEEE International Conference on Computer Design (ICCD), San Jose, CA (USA), October 2-5, 2005
69. The 8th Euromicro Conference on Digital System Design (DSD), Porto (Portugal), August 30th, September 3rd, 2005
70. The 6th Workshop on Complexity-Effective Design (WCED), in conjunction with the 32nd Annual International Symposium on Computer Architecture, Madison (WI), June 4-8, 2005
71. The 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS), Denver, CO (USA), April 4-8, 2005
72. The 14th International Conference on Compiler Construction (CC), Edinburgh (UK), April 4-8, 2005
73. 3rd Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO), San Jose, CA (USA), March 20-23, 2005
74. The 9th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT), held in conjunction with the 11th International Symposium on High-Performance Computer Architecture (HPCA), San Francisco (USA), February 12-16, 2005
75. 11th International Symposium on High-Performance Computer Architecture (HPCA), San Francisco (USA), February 12-16, 2005
76. Workshop on Memory Performance: Dealing with Applications, Systems and Architecture (MEDEA), in conjunction with the Int. Conference on Parallel Architectures and Compilation Techniques (PACT), Antibes Juan-Les Pins (France), 2004
77. 5th Int. Conference on Control, Virtual Instrumentation and Digital Systems, Mexico (Mexico), 2004
78. Ninth Asia-Pacific Computer Systems Architecture Conference, Beijing (China), 2004
79. 8th Int. Workshop on Software and Compilers for Embedded Systems (SCOPES), Amsterdam (The Netherlands), 2004
80. 2004 Euromicro Symposium on Digital System Design (DSD), Rennes (France), 2004
81. 18th Int. Conference on Supercomputing, Saint Malo (France), 2004
82. Workshop on Complexity-Effective Design (WCED), held in conjunction with the 31st Int. Symp. on Computer Architecture, Munich (Germany), 2004
83. International Parallel and Distributed Processing Symposium, Santa Fe (USA), 2004
84. 2nd Annual IEEE/ACM International Symposium on Code Generation and Optimization, San Jose (USA), 2004
85. 1st International Workshop on Embedded Computing, in conjunction with the 24th Int. Conf. on Distributed Computing Systems (ICDCS), Tokyo (Japan), 2004

86. ACM Symposium on Applied Computing (SAC), Nicosia (Cyprus), 2004
87. International Symposium on Performance Analysis of Systems and Software (ISPASS), Austin (USA), 2004
88. 8th Annual Workshop on Interaction between Compilers and Computer Architecture, held in conjunction with the 10th Int. Symposium on High-Performance Computer Architecture (HPCA), Madrid (Spain), 2004
89. 10th Int. Symposium on High-Performance Computer Architecture (HPCA), Madrid (Spain), 2004
90. 12th Euromicro Conference on Parallel, Distributed and Networked Based Processing, A Coruña (Spain), 2004
91. 36th Int. Symposium on Microarchitecture (MICRO), San Diego (USA), 2003
92. 21st Int. Conference on Computer Design, San Jose (USA), 2003
93. Workshop on Memory Performance: Dealing with Applications, Systems and Architecture (MEDEA), in conjunction with the Int. Conference on Parallel Architectures and Compilation Techniques (PACT), New Orleans (USA), 2003
94. 7th Int. Workshop on Software and Compilers for Embedded Systems (SCOPES), Vienna (Austria), 2003
95. 2003 Euromicro Symposium on Digital System Design (DSD), Antalya (Turkey), 2003
96. Workshop on Complexity-Effective Design (WCED), held in conjunction with the 30 th Int. Symp. on Computer Architecture, San Diego (USA), 2003
97. 30th Int. Symp. on Computer Architecture, San Diego (USA), 2003
98. 1st Annual IEEE/ACM Int. Symp. on Code Generation and Optimization, San Francisco (USA), 2003
99. 18th ACM Symp. on Applied Computing (SAC), Melbourne (USA), 2003
100. 7th Annual Workshop on Interaction between Compilers and Computer Architecture, held in conjunction with the 9th Int. Conference on High-Performance Computer Architecture (HPCA), Anaheim (USA), 2003
101. 9th Int. Conference on High-Performance Computer Architecture (HPCA), Anaheim (USA), 2003
102. 2003 Euromicro Conference on Parallel, Distributed and Networked-Based Processing, Genova (Italy), 2003
103. 35th Int. Symposium on Microarchitecture (MICRO), Istanbul (Turkey), 2002
104. Workshop on Memory Access Decoupled Architecture and Related Issues (MEDEA), in conjunction with the International Conference on Parallel Architectures and Compilation Techniques (PACT), Charlottesville (USA), 2002
105. 2002 International Conference on Computer Design, Freiburg (Germany), 2002
106. 2002 Euromicro Symposium on Digital System Design (DSD), Dortmund (Germany), 2002
107. Workshop on Complexity-Effective Design (WCED), held in conjunction with the 29th Int. Symp. on Computer Architecture, Anchorage (USA), 2002
108. 6th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT), in conjunction with the 8th Int. Symp. on High-Performance Computer Architecture, Cambridge (USA), 2002
109. Power Aware Computing Systems Workshop, in conjunction with the 8th Int. Symp. on High-Performance Computer Architecture, Cambridge (USA). 2002
110. 10th Euromicro Workshop on Parallel, Distributed and Network-based Processing, Las Palmas de Gran Canaria (Spain), 2002
111. Workshop on Memory Access Decoupled architecture and Related Issues (MEDEA), in conjunction with the International Conference on Parallel Architectures and Compilation Techniques (PACT), Barcelona (Spain), 2001
112. Workshop on Complexity-Effective Desing (WCED), in conjunction with the 28th Int. Symp. on Computer Architecture, Goteborg (Sweden), 2001
113. 34th. International Symposium on Microarchitecure (MICRO), Austin (USA), 2001
114. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Tucson (USA), 2001
115. 15th International Conference on Supercomputing (ICS), Sorrento (Italy), 2001
116. 2001 International Conference on Parallel Architectures and Compilation Techniques (PACT), Barcelona (Spain), 2001
117. 2001 Euromicro Symposium on Digital System Design (DSD), Warsaw (Poland), 2001

118. 5th. Ann. Workshop on Interaction between Compilers and Computer Architecture (INTERACT) in conjunction with HPCA-7, Monterrey (Mexico), 2001
119. 9th Euromicro Workshop on Parallel and Distributed Processing, Mantova (Italy), 2001
120. 4th Workshop on Multithreaded Execution, Architecture and Compilation, in conjunction with International Symposium on Microarchitecture (MICRO), Monterey, CA (USA), 2000
121. Memory Access Decoupling for Superscalar and Multiple Issue Architectures Workshop (MEDEA), in conjunction with PACT 2000, Philadelphia (USA), 2000
122. 3rd. Int. Conf. on Compilers, Architectures and Synthesis for Embedded Computing Systems, San Jose (USA), 2000
123. Workshop on Solving the Memory Wall, in conjunction with International Symposium on Computer Architecture (ISCA), Vancouver (Canada), 2000
124. The International Symposium on High Performance Computing, Tokyo (Japan), 2000
125. 26th Euromicro Conference - Symposium on Digital Systems Design (DSD), Maastricht (The Netherlands), 2000
126. 27th Ann. Int. Symposium on Computer Architecture (ISCA), Vancouver (Canada), 2000
127. 4th. Ann. Workshop on Interaction between Compilers and Computer Architecture (INTERACT) in conjunction with the 6th. Int. Symp. on High-Performance Computer Architecture, Toulouse (France), 2000
128. Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC) in conjunction with the 6th. Int. Symp. on High-Performance Computer Architecture, Toulouse (France), 2000
129. 8th. Euromicro Workshop on Parallel and Distributed Processing, Rhodos (Greece), 2000
130. Euromicro Workshop on Digital Systems Design (DSD), Milan (Italy), 1999
131. 7th. Euromicro Workshop on Parallel and Distributed Processing, Funchal (Portugal), 1999
132. Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC) in conjunction with the 5th. Int. Symp. on High-Performance Computer Architecture, Orlando (USA), 1999
133. 31st. ACM/IEEE Int. Symposium on Microarchitecture (MICRO), Dallas (USA), 1998
134. Euromicro Workshop on Digital Systems Design, Västeras (Sweden), 1998
135. 6th. Euromicro Workshop on Parallel and Distributed Processing, Madrid (Spain), 1998
136. Distributed Computer Communication Networks, Tel-Aviv (Israel), 1997
137. Euromicro Workshop on Computational Intelligence, Budapest (Hungary), 1997
138. 23rd Euromicro Conference, Budapest (Hungary), 1997
139. Distributed Computer Communication Networks, Tel-Aviv (Israel), 1996
140. 22nd Euromicro Conference, Prague (Czech Republic), 1996
141. 2nd. International Conference on Massively Parallel Computing Systems, Ischia (Italy), 1996
142. 4th Euromicro Workshop on Parallel and Distributed Processing, Braga (Portugal), 1996
143. 21st Euromicro Conference, Como (Italy), 1995
144. 2nd Euromicro Workshop on Parallel and Distributed Processing, Málaga (Spain), 1994

11. Comité Editorial de Revistas

1. Member of the Program Committee of the IEEE Micro Special Issue on Top Picks from the 2024 Computer Architecture Conferences, July-August 2025.
2. Member of the Program Committee of the IEEE Micro Special Issue on Top Picks from the 2023 Computer Architecture Conferences, July-August 2024.
3. Member of the Program Committee of the IEEE Micro Special Issue on Top Picks from the 2022 Computer Architecture Conferences, July-August 2023.
4. Member of the Program Committee of the IEEE Micro Special Issue on Top Picks from the 2021 Computer Architecture Conferences, May-June 2022.
5. Member of the Program Committee of the IEEE Micro Special Issue on Top Picks from 2013 Computer Architecture Conferences, May-June 2014.
6. Associate Editor of ACM Transactions on Parallel Computing, from 2012 to 2023.
7. Associate Editor of IEEE Computer Architecture Letters, from January 2010 to May 2014.
8. Co-Chair of Program Committee IEEE MICRO Special Issue on Top Picks from 2006 Computer Architecture Conferences, Jan.-Feb. 2007.
9. Member of Program Committee of the IEEE MICRO Special Issue on Top Picks from 2005 Computer Architecture Conferences, Jan.-Feb. 2006.
10. Associate Editor of the Journal IEEE Transactions on Computers, 2004-2009.
11. Associate Editor of the Journal ACM Transactions on Architecture and Code Optimization, 2003-2017.
12. Associate Editor of the Journal IEEE Transactions on Parallel and Distributed Systems, 2003-2008.
13. Member of the Editorial Board of the Journal of Embedded Computing, 2003-2012.
14. Member of the Editorial Board of the Special Edition about “Tools and Environments for Parallel Program Development” of the Journal of Systems Architecture, 1999.
15. Member of the Editorial Board of the Journal Novática, working as technical responsible for the Computer Architecture area, 1998-2002.
16. Member of the Editorial Board of the Special Edition about “Parallel Systems Engineering” of the Journal of Systems Architecture, 1996.
17. Member of the Editorial Board of the Journal Informática y Automática, working as technical responsible for the Computer Architecture area, 1992-2000.

12. Patentes Concedidas

(todas están actualmente en explotación)

[P.1] G. Savransky, R. Ronen and A. González, "System and Method of Reducing the Number of Copies from Alias Registers to Real Registers in the Commitment of Instructions". US patent number 7,024,542, issued 04/04/2006.

[P.2] P. Marcuello, A. González, H. Wang, J.P. Shen, P. Hammarlund, G.F. Hoflehner, P.H. Wang and S. S-W Liao, "Control-Quasi-Independent-Points Guided Speculative Multithreading", China patent number 03156069.5, issued 08/09/2006; China patent number 200310121592.4, issued 02/28/2007.

[P.3] P. Chaparro, J. González and A. González, "Temperature-Aware Steering Mechanism", Korea patent number 10-0634931, issued 10/10/2006; Taiwan patent number I285306, issued 08/11/2007; US patent number 7,330,983, issued 02/12/2008; China patent number 200510078948.X, issued 05/14/2008; European patent, pending, filed in November 12, 2013, filing number 13192451.6.

[P.4] J. González and A. González, "An Apparatus and Method for an Energy Efficient Clustered Micro-Architecture", US patent number 7,194,643, issued 03/20/2007.

[P.5] F. Latorre, J. González and A. González, "Register Allocation Technique", US patent number 7,313,675, issued 12/25/2007.

[P.6] G. Magklis, J. González and A. González, "Frequency and Voltage Scaling Architecture", US patent number 7,434,073, issued 10/07/2008; Great Britain patent number GB2432939, issued 01/21/2009; Germany patent number DE112005002416, issued 04/30/2009; China patent number ZL0580033614.9, issued 03/03/2010; Japan patent number 4,860,624, issued 11/16/2011.

[P.7] J. Abella, X. Vera, O. Unsal and A. González, "NBTI-Resilient Memory Cells with Nand Gates", US patent number 7,447,054, issued 11/04/2008; Korea patent number 10-1059062, issued 08/17/2011; Japan patent number 5095741, issued 09/28/2012; China patent number ZL200680055721.6, issued 02/06/2013; Germany patent, pending, filed in September 28, 2006, filing number DE112006004002T5.

[P.8] J. Sánchez, C. García, C. Madriles, P. Rundberg, P. Marcuello and A. González, "Selection of Spawning Pairs for a Speculative Multithreaded Processor", US patent number 7,458,065, issued 11/25/2008.

[P.9] F. Latorre, J. González and A. González, "Multithreaded Clustered Microarchitecture with Dynamic Back-End Assignment", US patent number 7,478,198, issued 01/13/2009.

[P.10] O. Ergin, O. Unsal, X. Vera and A. González, "Reducing the Soft Error Vulnerability of Stored Data", US patent number 7,558,992, issued 07/07/2009; Korean patent number 10-1001068, issued 12/07/2010.

[P.11] J. Abella, X. Vera, J. Carretero, A. Piñeiro and A. González, "Memory Content Inverting to Minimize NTBI Effects", US patent number 7,577,015, issued 08/18/2009.

[P.12] X. Vera, O. Ergin, O. Unsal and A. González, "Clustered Variations-Aware Microarchitecture", US patent number 7,600,145, issued 10/06/2009; Korean patent number 10-0971806, issued 07/15/2010; China patent number ZL200580051928.1, issued 11/02/2011.

[P.13] J. González and A. González, "Apparatus for an Energy Efficient Clustered Micro-Architecture", US patent number 7,657,766, issued 02/02/2010.

[P.14] A. González, Q. Cai, J. González, P. Chaparro, G. Magklis and R. Rakvic, "Meeting Point Thread Characterization", US patent number 7,665,000, issued 02/16/2010.

[P.15] X. Vera, J. Abella, J. González, A. Piñeiro, A. González and R. Ronen, "Selectively Protecting a Register File", US patent number 7,689,804, issued 03/30/2010.

[P.16] G. Magklis, J. González, P. Chaparro, Q. Cai and A. González, "Compressing Address Communications between Processors", US patent number 7,698,512, issued 04/13/2010.

[P.17] P. Chaparro, G. Magklis, J. González and A. González, "Leakage Power Estimation", GB patent number 2457752, issued 05/07/2010; US patent number 7,814,339, issued 10/12/2010; Korea patent number 10-1048751, issued 07/06/2011; China patent, pending, filed in June 30, 2006, filing number 200680054765.7; continuation to filing number 200680054765.7, pending, filed in June 30, 2006, filing number 201210363721.X; Japan patent, pending, filed in June 30, 2006, filing number 2009-510475.

[P.18] H. Wang, T. Aamodt, P. Marcuello, J.W. Stark, J.P. Shen, A. González, P. Hammarlund, G.F. Hoflehner, P.H. Wang and S. S-W Liao, "Speculative Multi-Threading for Instruction Prefetch and/or Trace Pre-Build", US patent number 7,814,469, issued 10/12/2010.

[P.19] X. Vera, O. Ergin, O. Unsal, J. Abella, A. González, "Detecting Soft Errors via Selective Re-execution", Korean patent number 10-0990591, issued 10/21/2010; US Patent number 8,090,996, issued 01/03/2012; China patent number ZL200680054141.5, issued 10/16/2013.

[P.20] X. Vera, O. Unsal, O. Ergin, J. Abella and A. González, "Enhancing Reliability of a Many-Core Processor", Japan patent number 4653841, issued 12/24/2010; US patent number 8,074,110, issued 12/06/2011; China patent number CN101390067A, issued 12/05/2012; continuation to patent number 8,074,110, Japan patent number 5328743, issued 08/02/2013.

[P.21] F. Latorre, J. González and A. González, "Multithreaded Clustered Microarchitecture with Dynamic Back-End Assignment", continuation to 7,478,198, US patent number 7,996,617, issued 08/09/2011.

[P.22] J. Moses, A. Piñeiro, D. Newell, E. Gibert, R. Iyer, J. Abella, J.M. Codina, R Illikkal, P. López, F. Latorre, S. Makineni and A. González, "Cache Sharing Based Thread Control", US patent number 7,895,415, issued 02/22/2011.

[P.23] Q. Cai, J. González, P. Chaparro, G. Magklis and A. González, "Thread Migration to Improve Power Efficiency in a Parallel Processing Environment", US patent number 7,930,574, issued 04/19/2011.

[P.24] C. Madriles, C. García Quiñones, P. Marcuello, J. Sánchez, F. Latorre and A. González, "Method, Apparatus and System Applied in A Cache Memory Coherence Protocol", China patent number ZL200680054734.1, issued 11/16/2011.

[P.25] C. Wilkerson, M. Khellah, V. De, M. Zhang, J. Abella, J. Carretero, P. Chaparro, X. Vera, A. González, "Disabling cache portions during low voltage operations", US Patent number 8,103,830, issued 01/24/2012.

[P.26] X. Vera, J. Abella, O. Unsal, O. Ergin and A. González, "Dynamically Estimating Lifetime of a Semiconductor Device", US patent number 8,151,094, issued 04/03/2012; China patent number ZL200580052138.5, issued 02/13/2013; second continuation to China patent number ZL200580052138.5, pending, filed in December 30, 2005, publication number CN103150221 A; continuation to China patent number ZL200580052138.5, pending, filed in December 30, 2005, publication number CN102831019 A; German patent number, pending, filed in December 30, 2005, publication number DE 11 2005 003 788T5.

[P.27] C. Madriles, P. Rundberg, J. Sánchez, C. García, P. Marcuello and A. González, "Multi-Version Register File for Multithreading Processors with Live-in Precomputation", US Patent number 8,166,282, issued 04/24/2012.

[P.28] Q. Cai, J. González, P. Chaparro, G. Magklis and A. González, "Thread Migration to Improve Efficiency in a Parallel Processing Environment", continuation to patent number 7,930,574, US Patent number 8,166,323, issued 04/24/2012.

[P.29] C. Madriles, C. García, P. Marcuello, J. Sánchez, F. Latorre and A. González, "Enabling Speculative State Information in a Cache Coherency Protocol", US patent number 8,185,700, issued 05/22/2012.

[P.30] F. Latorre, G. Magklis, E. Gibert, J.M. Codina and A. González, "Achieving Coherence Between Dynamically Optimized Code and Original Code", US patent number 8,190,652, issued 05/29/2012.

[P.31] E. Gibert, J.M. Codina, F. Latorre, A. Piñeiro, P. López and A. González, "Access of Register Files of Other Threads Using Synchronization", US patent number 8,261,046, issued 09/04/2012; Japan patent number 5283739, issued 06/07/2013; China patent, pending, filed in October 27, 2006, application number 200680056225.2.

[P.32] C. Wilkerson, M. Khellah, V. De, M. Zhang, J. Abella, J. Carretero, P. Chaparro, X. Vera, A. González, "Disabling cache portions during low voltage operations", continuation to patent number 8,103,830, US Patent number 8,291,168, issued 10/16/2012; Korea patent number 10-1252367, issued 04/02/2013; Taiwan patent number I420294, issued 12/21/2013; China patent number ZL200910222700.4, issued 09/25/2013; Brasil patent, pending, filed in September 23, 2009, filing number PI 0913782-3; Japan patent, pending, filed in September 23, 2009, filing number 2011-528093.

[P.33] A. González, C. Madriles, F. Latorre, R. Martinez, E. Gibert, P. López, A. Martinez and J.M. Codina, "Register Checkpointing Mechanism for Multithreading", European, Germany, Great Britain and Netherlands Patent number 2239657, issued 11/21/2012; Japan patent number 5242620, issued 04/12/2013; China patent, pending, filed in April 6, 2010, filing number 201010161083.4.

[P.34] X. Vera, J. Abella, J. Carretero and A. González, "Protecting Data Storage Structures from Intermittent Errors", US Patent number 8,352,812, issued 01/08/2013.

[P.35] X. Vera, O. Ergin, O. Unsal, J. Abella, A. González, "Detecting Soft Errors via Selective Re-Execution", continuation to Patent number 8,090,996, US Patent number 8,402,310, issued 03/19/2013.

[P.36] G. Magklis, J. González and A. González, "Frequency and Voltage Scaling Architecture", continuation to patent number 4860624, Japan patent number P5159931, issued 12/21/2012; continuation to patent number 7,434,073, US patent number 8,407,497, issued 03/26/2013.

[P.37] F. Latorre, J. González and A. González, "Multithreaded Clustered Microarchitecture with Dynamic Back-End Assignment", continuation to patents number 7,478,198 and 7,996,617, US patent number 8,423,716, issued 04/16/2013.

[P.38] J. Abella, X. Vera, J. Carretero, P. Chaparro and A. González, "Memory Apparatuses with Low Supply Voltages", US Patent number 8,477,558, issued 07/02/2013.

[P.39] F. Latorre, J.M. Codina, E. Gibert, P. López, C. Madriles, A. Martínez, R. Martínez, A González, "Systems, Methods, And Apparatuses to Decompose a Sequential Program into Multiple Threads, Execute Said Threads, and Reconstruct the Sequential Execution", Korea patent number 10-1292439, issued 07/26/2013; US patent number 8,909,902, issued 12/09/2014; Brazil patent, pending, filed in November 24, 2009, serial number PI0920541-1; China patent, pending, filed in November 24, 2009, serial number 200980139244.5; Japan patent, pending, filed in November 24, 2009, serial number 2011-536625.

[P.40] J. Abella, X. Vera and A. González, "Reducing Aging Effect on Registers", US patent number 8,578,137, issued 11/05/2013.

[P.41] P. Lopez, F. J. Sánchez, J. M. Codina, E. Gibert, F. Latorre, G. Magklis, P. Marcuello and A. González, "A Replacement Policy for Hot Code Detection", US patent number 8,612,698, issued 12/17/2013.

[P.42] G. Magklis, J. González and A. González, "Frequency and Voltage Scaling Architecture", second continuation to US patent number 7,434,073, US Patent number 8,689,029, issued 04/01/2014.

[P.43] H. Wang, T. Aamodt, P. Marcuello, J.W. Stark, J.P. Shen, A. González, P. Hammarlund, G.F. Hoflehner, P.H. Wang and S. S-W Liao, "Speculative Multi-Threading for Instruction Prefetch and/or Trace Pre-Build", continuation to US patent number 7,814,469, US Patent number 8,719,806, issued 05/06/2014.

[P.44] Q. Cai, J. González, P. Chaparro, G. Magklis and A. González, "Thread Migration to Improve Power Efficiency in a Parallel Processing Environment", second continuation to patent numbers 7,930,574 and 8,166,323, US Patent number 8,806,491, issued 08/12/2014.

[P.45] C. García Quiñones, J. Sánchez, C. Madriles, P. Marcuello and A. González, "Branch Pruning in Architectures with Speculative Support", US Patent Number 8,813,057, issued 08/19/2014.

[P.46] G. Magklis, J. González and A. González, "Frequency and Voltage Scaling Architecture", third continuation to US patent number 7,434,073, US Patent number 9,047,014, issued 06/02/2015.

[P.47] E. Gibert, F. Latorre, J.M. Codina, C. Gomez, A. González, M. Hyuseinova, C. Kotselidis, P. Lopez, M. Lupon, C. Madriles, G. Magklis, P. Marcuello, R. Martinez, A. Martinez, D. Ortega, D. Pavlou, K. Stavrou, G. Tournavitis and P. Xekalakis, "Support for Speculative Ownership Without Data", Korea Patent number 10-1529036, issued 06/16/2015; Japan Patent number JP-5771289 issued issued 08/26/2015; Patent Cooperation Treaty patent, pending, filed in December 29, 2011, filing number PCT/US11/067865; US patent, pending, filed in December 29, 2011, filing number 13/994,686; China patent, pending, filed in December 29, 2011, filing number 201180068658.0; Brasil patent, pending, filed in December 29, 2011, filing number BR 11 2013 019106-6; Taiwan patent, pending, filed in December 26, 2012, filing number 101150125.

[P.48] C. Wilkerson, M. Khellah, V. De, M. Zhang, J. Abella, J. Carretero, P. Chaparro, X. Vera, A. González, "Disabling cache portions during low voltage operations", second continuation to US Patent number 8,103,830, US Patent number 9,678,878, issued 06/13/2017.

[P.49] K. Stavrou, E. Gibert, J.M. Codina, C. Gomez Requena, A. González, M. Hyuseinova, C. Kotselidis, F. Latorre, P. Lopez, M. Lupon, C. Madriles, G. Magklis, P. Marcuello, A. Martinez, R. Martinez, D. Ortega, D. Pavlou, G. Tournavitis and P. Xekalakis, "Managed Instruction Cache Prefetching", US Patent number 9,811,341, issued 11/07/2017.

[P.50] P. Lopez, C. Madriles, A. Martinez, R. Martinez, J.M. Codina, E. Gibert, F. Latorre, A. González, "Utilization of Register Checkpointing Mechanism with Pointer Swapping to Resolve Multithreading Mis-speculations", US Patent number 9,940,138, issued 04/10/2018.

[P.51] R. Martínez, E. Gibert, P. Lopez, M. Torrents, P. Xekalakis, G. Tournavitis, K. Stavrou, D. Pavlou, D. Ortega, A. Martinez, P. Marcuello, G. Magklis, J.M. Codina, C. Gomez, A. González, M. Hyuseinova, C. Kotselidis, F. Latorre, M. Lupon and C. Madriles, "Propagating a Prefetching Profile Bit from a Prefetch Queue to a Data Cache to Indicate that a Line Was Prefetched in Response to an Instruction within a Code Region", US Patent number 10,013,326, issued 07/03/2018.

[P.52] C. Wilkerson, M. Khellah, V. De, M. Zhang, J. Abella, J. Carretero, P. Chaparro, X. Vera, A. González, "Disabling cache portions during low voltage operations", third continuation to US Patent number 8,103,830, US Patent number 10,528,473, issued 01/07/2020.

[P.53] F. Latorre, J.M. Codina, E. Gibert, P. López, C. Madriles, A. Martínez, R. Martínez and A. González, "Merging level cache and data cache units having indicator bits related to speculative execution", US Patent number 10,621,092, issued 04/14/2020.

13. Premios y Distinciones

1. HiPEAC award for his paper “K-D Bonsai: ISA Extensions to Compress K-D Trees for Autonomous Driving Tasks” published in International Symposium on Computer Architecture, 2023.
2. HiPEAC award for his paper “DTexL: Decoupled Raster Pipeline for Texture Locality” published in International Symposium on Microarchitecture, 2022.
3. HiPEAC award for his paper “TCOR: A Tile Cache with Optimal Replacement” published in International Symposium on High-Performance Computer Architecture, 2022.
4. ACM Fellow since December 2020 “for contributions to the design of energy-efficient and resilient computer architectures”.
5. ACM Senior Member since May 2020 “for technical leadership, and technical and professional contributions”.
6. ICREA Academia Award 2019 given by the Catalan Institution for Research and Advanced Studies to reward professors who excel on their research activity.
7. HiPEAC award for his paper “Neuron-Level Fuzzy Memoization in RNNs” published in International Symposium on Microarchitecture, 2019.
8. HiPEAC award for his paper “SCU: A GPU Stream Compaction Unit for Graph Processing” published in International Symposium on Computer Architecture, 2019.
9. HiPEAC award for his paper “Early Visibility Resolution for Removing Ineffectual Computations in the Graphics Pipeline” published in International Symposium on High-Performance Computer Architecture, 2019.
10. HiPEAC award for his paper “Rendering Elimination: Early Discard of Redundant Tiles in the Graphics Pipeline” published in International Symposium on High-Performance Computer Architecture, 2019.
11. HiPEAC award for his paper “The Dark Side of DNN Pruning” published in International Symposium on Computer Architecture, 2018.
12. HiPEAC award for his paper “Computation Reuse in DNNs by Exploiting Input Similarity” published in International Symposium on Computer Architecture, 2018.
13. HiPEAC award for his paper “A Novel Register Renaming Technique for Out-of-Order Processors” published in International Symposium on High-Performance Computer Architecture, 2018.
14. Special Quality Teaching Merits distinction for his teaching activity at UPC in the period 2008-2016.
15. HiPEAC award for his paper “UNFOLD: A Memory-Efficient Speech Recognizer Using On-the-Fly WFST Composition” published in International Symposium on Microarchitecture, 2017.
16. HiPEAC award for his paper “MeRLiN: Exploiting Dynamic Instruction Behavior for Fast and Accurate Microarchitecture Level Reliability Assessment” published in International Symposium on Computer Architecture, 2017.
17. Intel-Altera Heterogeneous Architecture Research Platform (HARP) 2.0 award, November 2016.
18. HiPEAC award for his paper “An Ultra Low-Power Accelerator for Automatic Speech Recognition” published in International Symposium on Microarchitecture 2016.
19. HiPEAC award for his paper “Ultra-Low Power Render-Based Collision Detection for CPU/GPU Systems” published in International Symposium on Microarchitecture 2015.
20. Intel-Altera Heterogeneous Architecture Research Platform (HARP) award, June 2015.
21. Honorable Mention in IEEE Micro Top Picks 2014 for his paper “Avoiding Core's DUE and SDC via Acoustic Wave Detectors and Tailored Error Containment and Recovery”, published in the Proc. of the 41st Int. Symp on Computer Architecture.
22. ICREA Academia Award 2014 given by the Catalan Institution for Research and Advanced Studies to reward professors who excel on their research activity.
23. Best Paper Award candidate at the Int. Conf. on Computer Design, 2014 for iRMW: A Low-Cost Technique to Reduce NBTI-Dependent Parametric Failures in L1 Caches” by Shrikanth Ganapathy, Ramon Canal, Antonio Rubio and Antonio González.

24. His paper "A data cache with multiple caching strategies tuned to different types of locality" has been selected for inclusion in the "25 years of International Conference on Supercomputing". This volume includes 35 out of approximately 1800 papers published in the International Conference on Supercomputing proceedings between 1987 and 2011 and is published by ACM. June 2014.
25. IEEE Fellow since January 2014 “for contributions to the design of energy-efficient and resilient processor architectures”.
26. Inducted into the “ACM/IEEE ISCA Hall of Fame” (http://pages.cs.wisc.edu/~arch/www/iscabibhall.html/), 2013.
27. HiPEAC award for his paper “Deconfigurable Microprocessor Architectures for Silicon Debug Acceleration” published in International Symposium on Computer Architecture 2013.
28. “Rey Jaime I Award” in the area of New Technologies, given by the Valencian Foundation for Advanced Studies, for his contributions to research and scientific development in Computer Architecture, June 2013.
29. Intel Quality Award received as a director of Intel Labs Barcelona, 2012.
30. UPC special doctoral award as advisor of the PhD theses “Managing Dynamic Non-Uniform Cache Architectures” (2011) and “Adaptive and Low-Complexity Microarchitectures for Power Reduction” (2005).
31. HiPEAC award for his paper “Accelerating Microprocessor Silicon Validation by Exposing ISA Diversity” published in International Symposium on Microarchitecture 2011.
32. “2009 Aritmel National Award of Informatics to the Computer Engineer of the Year”, given by the Spanish Scientific Society of Informatics.
33. Special Quality Teaching Merits distinction for his teaching activity at UPC in the period 2001-2008.
34. Inducted into the “IEEE HPCA Hall of Fame” (http://ieeetcca.org/awards/hpca-hall-of-fame/), 2005.
35. Duran Farell Award for Research in Technology, May 2008.
36. Best Paper Award at the Int. Conf. on Computer Design, 2004 for “Thermal-Aware Clustered Microarchitectures”, by Pedro Chaparro, José González, Antonio González.
37. “Most Outstanding Work in R&D” award from the journal ComputerWorld, given to Intel-UPC Labs. Received as director of the center. Year 2003.
38. Best Student Paper Award at the Int. Conf. on Parallel Processing (ICPP) 2002 for “Hardware Schemes for Early Register Release”, by Teresa Monreal, Victor Viñals, Antonio González and Mateo Valero.
39. Rosina Ribalta award to the best Ph.D. project in the area of Information Technology and Communications, for the Ph.D. project “The Subscalar Microarchitecture for Ultra-Low Power”. Received as advisor of the project. June 2001.
40. Inducted into the “IEEE/ACM MICRO Hall of Fame” (http://newsletter.sigmicro.org/micro-hof.txt/view), 2000.
41. Best Student Paper award at the 6th International Symposium on High-Performance Computer Architecture along with his students Ramon Canal and Joan Manuel Parcerisa for their paper “Dynamic Cluster Assignment Mechanisms”, Jan. 2000.
42. IBM Faculty Partnership Award, 2000.
43. "Fundación Universidad-Empresa" award to laureate the achievements of European University Departments in the European ESPRIT framework. Received as a member of the Computer Architecture Department at UPC, 1993.
44. “Best Spanish student in computer engineering graduating in 1986”, presented by the Spanish Ministry of Education.

14. Comités de Confianza

- Member of the IEEE/ACM International Symposium on Microarchitecture Test of Time Award committee since 2021.
- Member of the ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award committee since 2019 until 2021, being chair of the committee in 2020.
- Chair of the ACM SIGARCH/IEEE CS TCCA Influential ISCA Paper Award selection committee, 2018
- Member of the Communications of ACM Research Highlights paper selection committee in 2017.
- Member of the IEEE Computer Society Awards committee in 2016.
- Member of the ACM Awards committee in 2016.
- Member of the High Consulting Counsel for R+D+I of the Presidency of the Valencian Government since Oct. 2014.
- Member of the National Committee for Evaluating Research Activity (CNEAI) since February 2014 to December 2016, being chair of the committee in 2016.
- Member of the ACM/IEEE Eckert-Mauchly Award committee since 2014 to 2016, being chair of the committee in 2016.
- Member of the Executive Committee of the IEEE Technical Committee in Computer Architecture since 2015 to 2023.
- Executive Vice-Chair of the IEEE Technical Committee in Computer Architecture since 2010 to 2015.
- Member of the Award Committee of the 7th Award to Young Researchers of Murcia (Spain), 2010.
- Member of the Grandes Usuarios de Computación Committee (Committee of Major Computing Users) of the Supercomputing Center of Catalonia (CESCA) since 2002 to 2008.
- Member of the Board of Directors of the European Association for Microprocessing and Microprogramming (Euromicro), from 1993 to 1999.
- Member of the Parallel Processing Network of the European Research Consortium for Informatics and Mathematics (ERCIM), from 1994 to 1996.

15. Cargos Universitarios

1. Miembro de la Comisión de Evaluación y Selección de Personal Académico de la UPC (CSAPDIU) desde mayo de 2016 hasta febrero de 2021.
2. Director del Centro de Investigación Intel-UPC Barcelona desde febrero de 2002 hasta mayo de 2014.
3. Miembro de la Junta General de Personal de la UPC desde enero de 2001 hasta junio de 2002.
4. Miembro suplente del Comité de Selección del Departamento de Arquitectura de Computadores durante los años 2001/2002 y 2002/2003.
5. Miembro del Comité de Evaluación Global del Departamento de Arquitectura de Computadores de febrero a julio de 2001.
6. Miembro del Comité de Movilidad del Departamento de Arquitectura de Ordenadores desde febrero de 2001 hasta febrero de 2002.
7. Miembro de la Comisión de Evaluación Académica de la FIB desde marzo de 2003 hasta junio de 2010.
8. Secretario del Departamento de Arquitectura de Ordenadores de septiembre a noviembre de 2000.
9. Miembro del Comité de Evaluación Docente del Departamento de Arquitectura de Computadores de 1995 a 1998 y de febrero a julio de 2001.
10. Coordinador del Departamento de Arquitectura de Computadores para la evaluación de la investigación en la UPC (puntos PAR) de 1994 a 2002.
11. Representante del Departamento de Arquitectura de Computadores en los cursos de formación para profesores en el ICE, 1994 a 1996.
12. Representante de la UPC en AEDIMA y ERCIM de 1993 a 1996.
13. Miembro del Comité de Evaluación Curricular de la Escuela de Ingeniería Informática de la UPC de 1992 a 1995.
14. Miembro de la Comisión Permanente de la Escuela de Ingeniería Informática de la UPC desde enero de 1992, de diciembre de 1992 a 1995, y de febrero a julio de 2001.
15. Miembro del Consejo del Departamento de Arquitectura de Ordenadores de 1992 a 1997, y de septiembre a noviembre de 2000.
16. Miembro del Comité de Evaluación de Alumnos de la Escuela de Ingeniería Informática de la UPC de diciembre de 1990 a 1995.
17. Responsable de Planes de Estudios en el Departamento de Arquitectura de Computadores de 1989 a 1992 y de febrero a agosto de 2001.
18. Miembro de la Junta de Escuela de Ingeniería Informática de la UPC de 1986 a 1995 y de febrero a julio de 2001.
19. Miembro del Consejo de Departamento de Arquitectura de Computadores de la UPC desde octubre de 1986.

16. Otras Actividades

16.1. Revisor de Libros

- Revisor de la traducción al español del libro "Computer Architecture. A Quantitative Approach", by J.L. Hennessy and D.A. Patterson, Morgan Kaufmann Publishers. Translation published by McGraw Hill.
- Revisor de la traducción al español del libro "Principios de Diseño Digital", by Daniel D. Gajski, published by Prentice Hall.

16.2. Evaluación de Proyectos de Investigación

- Member of US panel to assess research proposals of the Computing Processes and Artifacts program of the USA National Science Foundation, 2007.
- Evaluador habitual de proyectos de investigación y desarrollo nacionales y europeos.

16.3. Proyectos Docentes

- Lecturer at the Master of Science in Embedded System Design and Master of Advanced Studies in Embedded System Design of the AlaRI Research Institute of the University of Lugano (Switzerland), from 2001 to 2014.
- UPC Coordinator in the ANTITESYS Project (IST-2001-34370) for the creation of a training network on embedded systems, from 2002 to 2004.
- UPC Coordinator of the Coopernet Project (EU Alpha Program) for the exchange of PhD students (1996-97).
- Representative of the Computer Architecture Department and tutor of several participants at the ICE training courses taking place during the courses 1994-1995 and 1995-1996.
- Coordination of UPC participation in the ERASMUS ICP-94-D-4001/11 project, together with the University of Hannover (Germany), the University of Crete (Greece) and the University of Bristol (UK).

16.4. Estancias en Otras Instituciones

- Microprocessor Research Labs – Intel Corporation, Santa Clara, CA (USA). Collaboration in Processor Microarchitecture Research. July 20 to November 30, 2001.
- Università di Bologna-Bertinoro (Italy), as a teacher of the PhD program in Computer Science at the Science School. May 21-28, 2000.
- Department of Electrical and Computer Engineering of the University of Wisconsin at Madison (USA). Collaboration in Speculative Microarchitectures. May 1-16, 1999.
- Department of Computer Science of the University of Edinburgh. Collaboration in the area of cache memory architectures to reduce conflict misses. August 1996.